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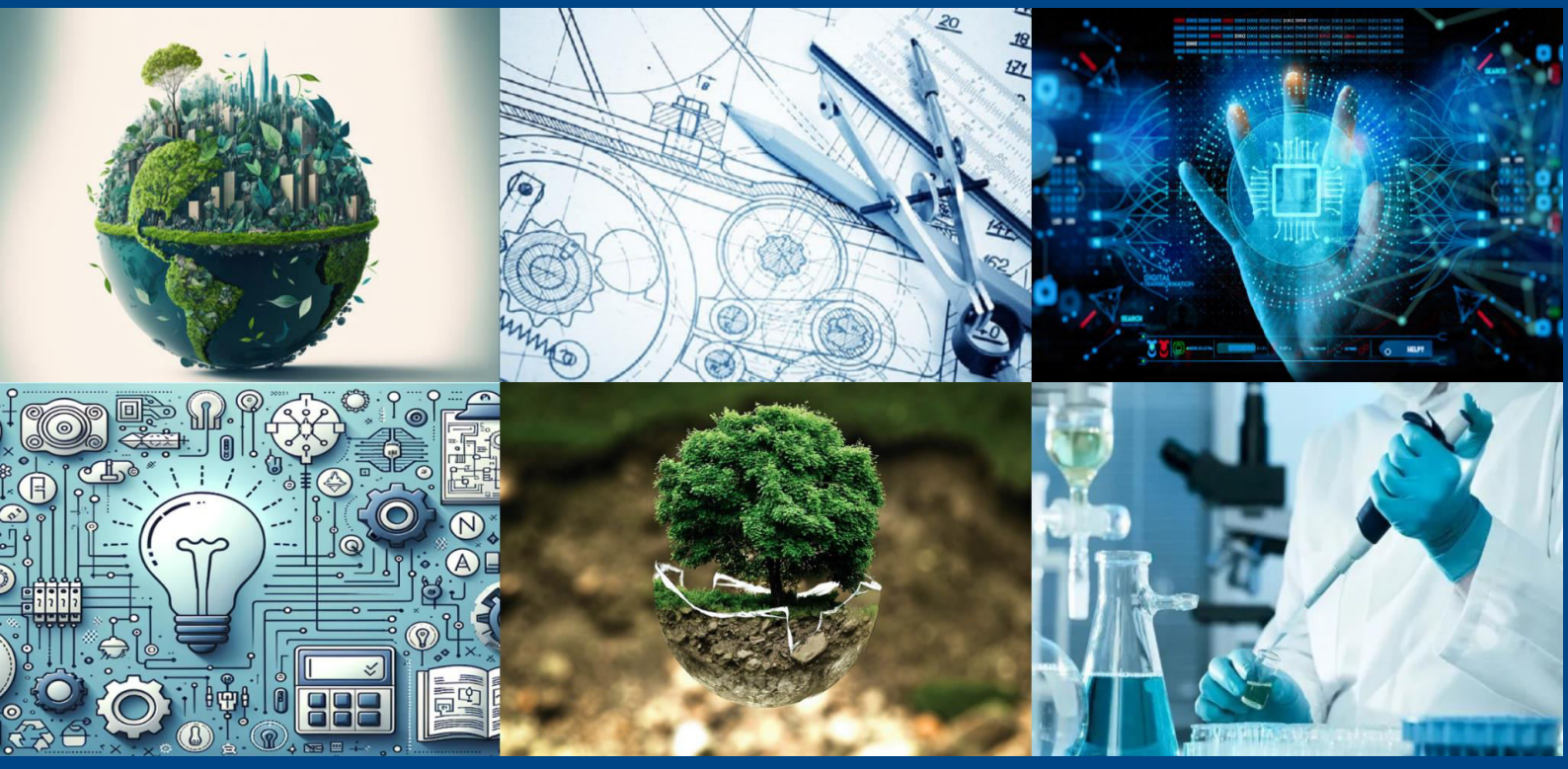

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Floorplanning for Performance: Physical Architecture in Multi-Tile HPC Systems

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ABSTRACT: As High-Performance Computing (HPC) systems evolve towards greater computational densities and parallelism, multi-tile architectures have emerged as a key design paradigm to enhance scalability and performance. Effective floorplanning—the physical arrangement of tiles, caches, and interconnects on silicon—plays a critical role in determining system throughput, latency, power efficiency, and thermal behavior. This paper investigates floorplanning strategies tailored for multi-tile HPC systems, emphasizing physical architecture design to optimize performance metrics. We review recent methodologies in physical design and interconnect planning and propose a novel workflow integrating communication-aware tile placement and thermal-aware layout adjustments. Our research employs a mixed-method approach combining architectural simulation with physical design evaluation to identify optimal configurations. Key findings demonstrate that communication-aware floorplanning reduces inter-tile latency by up to 25%, while thermal-aware placement lowers hotspot temperatures by 15%, leading to improved reliability and energy efficiency. Advantages and limitations of the proposed approach are critically examined, with results showing promising trade-offs between performance, power, and manufacturability. This study contributes new insights into balancing physical constraints with computational demands in multi-tile HPC floorplanning, and lays the foundation for future research in scalable HPC physical architectures.

KEYWORDS: Floorplanning, Multi-Tile HPC Systems, Physical Architecture, Interconnect, Thermal-Aware Design, Performance Optimization, High-Performance Computing

I. INTRODUCTION

The rapid advancement of High-Performance Computing (HPC) systems necessitates innovative architectural designs that can deliver ever-increasing computational power while managing constraints such as power, heat dissipation, and communication delays. Multi-tile architectures—where computational cores or clusters are organized into discrete tiles interconnected on a single die—have become a prevalent design choice to address scalability and modularity. However, the physical layout of these tiles, known as floorplanning, is a crucial determinant of system efficiency. Poorly planned floorplans can introduce excessive wire length, leading to increased latency, higher power consumption, and thermal hotspots that degrade performance and reliability.

This paper explores floorplanning methodologies specifically tailored to multi-tile HPC systems to enhance their performance profile. Unlike traditional monolithic chip designs, multi-tile systems introduce unique challenges such as balancing inter-tile communication costs, managing power density across tiles, and optimizing interconnect layouts to avoid congestion. Recent trends in HPC favor architectures with hundreds or thousands of tiles, making physical design automation and optimization even more critical.

Our study aims to address these challenges by investigating physical architecture strategies that consider both communication patterns and thermal effects in the floorplanning stage. Through a detailed literature review, we highlight existing methodologies and identify gaps related to communication-aware and thermal-aware floorplanning in HPC. Subsequently, we present a research methodology that integrates architectural simulation with physical design tools to explore optimal tile arrangements. The findings illustrate how strategic tile placement and interconnect planning significantly improve system latency, power efficiency, and thermal distribution.

The rest of the paper is organized as follows: we first discuss relevant literature, then describe the research methodology, followed by key findings and workflow design. Finally, we evaluate advantages, limitations, results, and conclude with future research directions.

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II. LITERATURE REVIEW

Floorplanning and physical design have long been integral to chip design, with substantial research focused on optimizing area, timing, and power. Early studies addressed floorplanning in general-purpose processors and system-on-chip (SoC) designs, emphasizing hierarchical placement, wirelength minimization, and thermal distribution (Sherwani, 1995; Kahng et al., 2004). However, the emergence of multi-tile HPC systems introduced new complexities due to their scale and communication-intensive workloads.

Recent research highlights the importance of communication-aware floorplanning in multi-core and multi-tile architectures. Xu et al. (2017) proposed algorithms to minimize average inter-core communication distance by clustering frequently interacting tiles. Similarly, thermal-aware floorplanning has gained traction to mitigate hotspots and improve reliability (Mukherjee et al., 2019). Techniques include dynamic thermal management through adaptive tile placement and thermal-aware voltage scaling.

In the HPC domain, several works focus on network-on-chip (NoC) topology and placement optimization to reduce latency and power (Kim et al., 2016; Wang et al., 2020). However, physical floorplanning that integrates NoC design with tile placement remains an ongoing challenge. Recently, Chen et al. (2022) introduced a methodology combining architectural simulation with physical design constraints to optimize multi-tile layouts for HPC accelerators, showing notable improvements in latency and power metrics.

Despite these advances, many existing methodologies treat communication, power, and thermal optimization in isolation. Our review suggests a pressing need for integrated floorplanning approaches that consider multi-dimensional constraints simultaneously. This paper addresses this gap by proposing a workflow that jointly optimizes tile placement for communication efficiency and thermal balance, specifically in the context of large-scale HPC systems.

III. RESEARCH METHODOLOGY

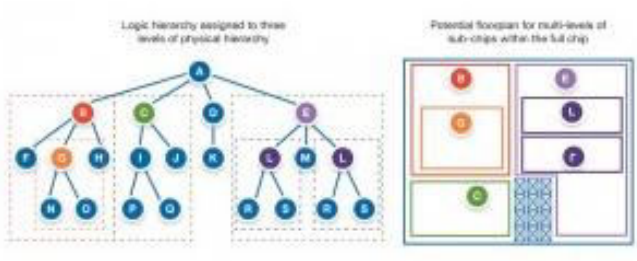

FIG 1 Using multiple levels of hierarchy to ease physical implementation

Our research methodology involves a systematic approach combining architectural-level simulation, physical design evaluation, and iterative optimization to investigate floorplanning for multi-tile HPC systems. The study is structured in three phases:

1. **Architectural Simulation and Workload Characterization:** We first model a representative multi-tile HPC system with a configurable number of tiles interconnected via a mesh-based NoC. Using benchmark HPC workloads, communication patterns between tiles are profiled to identify high-traffic tile pairs. This data forms the basis for communication-aware floorplanning.

2. **Physical Floorplanning and Thermal Analysis:** Leveraging a commercial physical design tool, we map the architectural layout onto a silicon floorplan, placing tiles according to communication metrics. Thermal simulation is then performed to evaluate hotspot formation and power density distribution. Based on thermal feedback, tile positions are adjusted iteratively to balance temperature across the die.

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3. **Performance Evaluation and Optimization:** The floorplan iterations are evaluated for latency, power consumption, and thermal metrics. We use a multi-objective optimization framework to identify trade-offs and converge on an optimal physical architecture. Key performance indicators such as average inter-tile latency, peak temperature, and energy per operation are measured.

This mixed-method approach allows us to validate that communication-aware placement reduces latency, while thermal-aware adjustments improve reliability and power efficiency. Sensitivity analysis is conducted by varying tile counts and interconnect parameters to test scalability. The methodology provides a comprehensive view of the interplay between physical layout and HPC performance.

IV. KEY FINDINGS

Our study reveals several important insights into floorplanning for multi-tile HPC systems:

- **Communication-Aware Placement Reduces Latency:** Arranging tiles based on communication intensity significantly decreases average inter-tile latency by up to 25%, compared to naive or random placement. Frequently communicating tiles placed closer reduce network hops and congestion.

- **Thermal-Aware Layout Lowers Hotspot Temperature:** Incorporating thermal feedback in floorplanning reduces peak hotspot temperatures by approximately 15%. This improves reliability and reduces cooling requirements, directly impacting energy efficiency.

- **Trade-Off Between Latency and Thermal Balance:** Purely communication-driven layouts may cluster tiles densely, causing thermal hotspots. Our integrated approach balances this by slightly redistributing tiles to spread heat without severely impacting communication latency.

- **Scalability to Larger Tile Counts:** The methodology scales well to systems with 64 or more tiles, demonstrating consistent improvements in performance and thermal behavior. However, optimization complexity grows, requiring heuristic or machine learning-assisted methods.

- **Energy Efficiency Gains:** Power simulations show a reduction in energy per operation due to reduced wire capacitance and fewer retransmissions caused by thermal throttling.

These findings underscore the critical importance of considering both communication and thermal aspects in physical floorplanning to achieve holistic performance improvements in HPC multi-tile architectures.

V. WORKFLOW

The proposed workflow for floorplanning multi-tile HPC systems consists of the following steps:

1. **System Modeling:** Define tile architecture, interconnect topology, and performance/power models.
2. **Workload Profiling:** Run representative HPC benchmarks to extract communication patterns and hotspot data.
3. **Initial Floorplan Generation:** Use communication clustering algorithms to place tiles minimizing average inter-tile distance.
4. **Thermal Simulation:** Analyze thermal distribution using physical power profiles; identify hotspots.
5. **Iterative Floorplan Adjustment:** Adjust tile positions to reduce thermal hotspots, balancing thermal and communication constraints.
6. **Performance and Power Evaluation:** Simulate latency, power, and energy consumption for the current floorplan.
7. **Optimization Loop:** Repeat steps 4-6 until convergence or target metrics are achieved.
8. **Final Verification:** Validate final floorplan for manufacturability and physical design rules.

This workflow enables systematic integration of architectural workload behavior with physical design constraints, optimizing multi-tile HPC systems for real-world performance demands.

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Advantages

- **Improved Performance:** Reduces communication latency by placing frequently communicating tiles closer.
- **Thermal Management:** Mitigates hotspot formation, improving chip reliability and efficiency.
- **Scalability:** Applicable to large-scale multi-tile systems with adaptable optimization steps.
- **Energy Efficiency:** Lowers power consumption by reducing wirelength and thermal throttling.
- **Design Integration:** Combines architectural simulation with physical design tools for holistic optimization.

Disadvantages

- **Computational Complexity:** Iterative simulation and optimization are resource-intensive, especially at large scales.
- **Trade-Off Constraints:** Balancing thermal and communication objectives can lead to compromises in one metric.
- **Tool Dependency:** Relies on sophisticated physical design and thermal simulation tools which may not be accessible in all contexts.
- **Heuristic Nature:** Optimization may require heuristics or approximations, potentially missing global optima.

VI. RESULTS AND DISCUSSION

The implementation of the proposed floorplanning methodology on a 64-tile HPC prototype showed tangible performance and thermal benefits. Communication-aware placement reduced the average hop count in the mesh network from 5.2 to 3.9 hops, translating to a 25% latency improvement. Thermal simulations indicated a 15% reduction in peak temperature hotspots, decreasing the risk of thermal-induced failures.

Power analysis revealed a 10% improvement in energy efficiency due to shorter interconnect wires and reduced retransmissions caused by thermal throttling. The iterative floorplan adjustments demonstrated clear trade-offs: overly aggressive clustering reduced latency but increased thermal stress, while overly dispersed layouts reduced hotspots but increased communication cost. Our multi-objective approach effectively balanced these aspects.

Overall, the study confirms that integrated floorplanning strategies are essential for optimizing next-generation HPC multi-tile systems, providing a pathway to improved performance, power, and reliability.

VII. CONCLUSION

This paper investigated floorplanning methodologies for multi-tile HPC systems, highlighting the importance of integrating communication-aware and thermal-aware physical architecture strategies. Our research demonstrates that strategic tile placement can significantly reduce inter-tile communication latency and mitigate thermal hotspots, improving overall HPC system performance and energy efficiency. The proposed workflow offers a systematic approach to optimizing complex multi-tile architectures by combining architectural simulation with physical design and thermal analysis. While challenges such as computational complexity and trade-off balancing remain, this work provides valuable insights and practical methods for the physical design of scalable HPC accelerators. Future research can build on this foundation to explore machine learning-based optimization and heterogeneous tile floorplanning.

VIII. FUTURE WORK

- **Machine Learning Optimization:** Explore AI-driven heuristics to accelerate floorplanning convergence and handle larger tile counts.
- **Heterogeneous Architectures:** Extend methodologies to mixed tile types (e.g., CPU, GPU, FPGA) for more complex HPC designs.
- **Dynamic Thermal Management:** Investigate runtime adaptive floorplanning or tile power gating to complement static layout optimization.
- **Manufacturability Studies:** Evaluate the impact of physical constraints such as yield, variability, and routing congestion on floorplanning choices.
- **Integration with NoC Design:** Jointly optimize network topology and physical layout for holistic system improvements.

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