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Design of High Performance Instrumentation Amplifier Employing Pseudo-Differential Inverter Using Header Transistor

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ABSTRACT: Inverter based Instrumentation Amplifier provides low power consumption and less area. In Conventional, the Inverter is based on Single Ended topology. The design of Instrumentational Amplifier based on SE topology offers low CMRR which is most disadvantage in this structure.In this project, a modified structure of Instrumentational amplifier in Pseudo Differential inverter topology is designed by inserting an additional transistor which is termed as Header transistor. This concept is relating to one of the low power techniques in advanced technologies which is Power Gating approach. Although power gating has many configurations individually, here presenting the configuration of header transistor. This entire structure is modified in Tanner EDA employing respective library files.

KEYWORDS: Instrumentational Amplifier, Common Mode Rejection Ratio(CMRR), Amplifier, Single Ended topology.

I. INTRODUCTION

Neurological disorder is one of the leading cause of death and disability. Sensing and recording neural signal become increasingly prevalent to extract the vital signs for diagnosis and treatment.A key enabling technology to support future clinical research in this healthcare topic is the wearable and implantable sensing system able to simultaneously record multiple neurological activities with a long lifetime battery capacity.The design of Instrumentational Amplifier based on SE topology offers low CMRR which is most disadvantage in this structure.In instrumentation amplifiers, common-mode rejection ratio (CMRR) is an essential parameter that reflects the ability to reject any unwanted common-mode signals that are present at the input. It is crucial to have a high CMRR to remove the common-mode interference from the environment.In this project, a modified structure of Instrumentational amplifier in Pseudo Differential inverter topology is designed by inserting an additional transistor which is termed as Header transistor.

II. EXISTING METHOD

The PD inverters are implemented to replace the A1 and A2 at the first stage. Capacitor C0 is reused at first stage. The common-mode output at the first stage is evaluated and the feedback is applied via the control terminal of PD inverter. To compare with the SE inverter-based IA, the second stage of both SE and PD inverter-based IA is the same. The gain of the second stage is unity. The supply voltage of the inverters and amplifier A3 is standard, and the bulk terminals of the transistor are connected to the appropriate rails.

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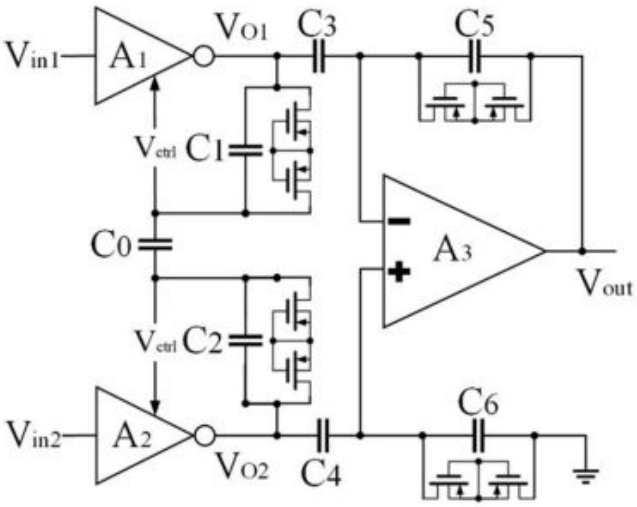

Figure.2.1Schematic of Existing Instrumentational Amplifier

Vin and Vout are the input and output terminal of the inverter. Vctrl is the pseudo input terminal in parallel with Vin (MN1, MN2 and MP1, MP2). PD effectively sums the outputs for Vin and Vctrl. The width of the input transistors is half of SE input transistor and the length is the same. With respect to the SE inverter, this topology requires no significant increase of the current or power, as the active load is reused by both input and pseudo input terminal. Associate with Fig. , the outputs of the PD inverter, VO1 and VO2, are used to dynamically eliminate CMI via the pseudo input terminal (Vctrl).

Disadvantages:

Slow performance

Power consumption is high

III. PROPOSED METHOD

This proposed methodology describes the necessity of low power techniques and also the importance of power gating techniques. Finally provides the detailed description of proposed structure of instrumentational amplifier using one of the power gating topology of header transistor. Here, the power gating approach is applied to the block of operational amplifier which remains the inverter in Pseudo differential topology.

Working of Power gating technique:

Power gating is a technique used in VLSI design to reduce power consumption in digital circuits by selectively turning off power to idle circuit blocks. One commonly used approach for power gating is using a header transistor.In this technique, a header transistor is added to the circuit, which acts as a switch to turn off the power supply to the idle circuit blocks. When the header transistor is turned off, it disconnects the power supply from the idle circuit blocks, effectively turning them off and reducing their power consumption to near-zero levels.By doing so, it enables designers to improve performance, and increase the reliability of digital circuits.

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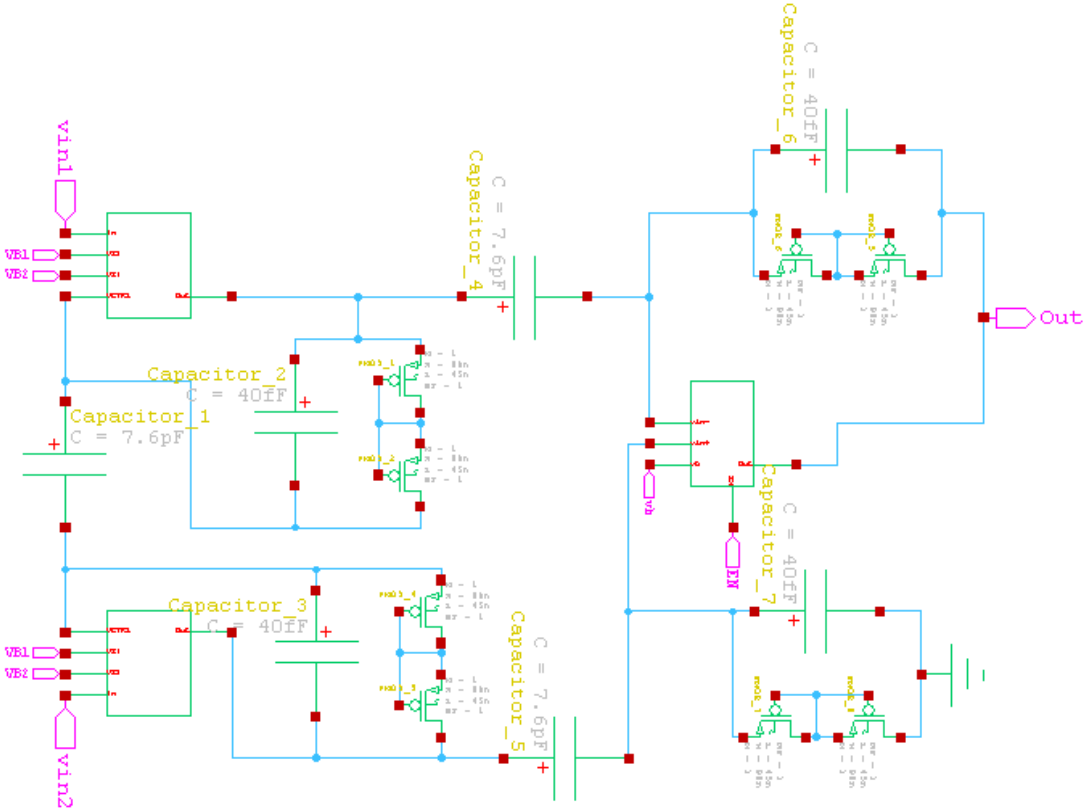

Figure.3.1Proposed schematic of Instrumentational Amplifier

IV. RESULT & ANALYSIS

RTL SCHEMATIC:

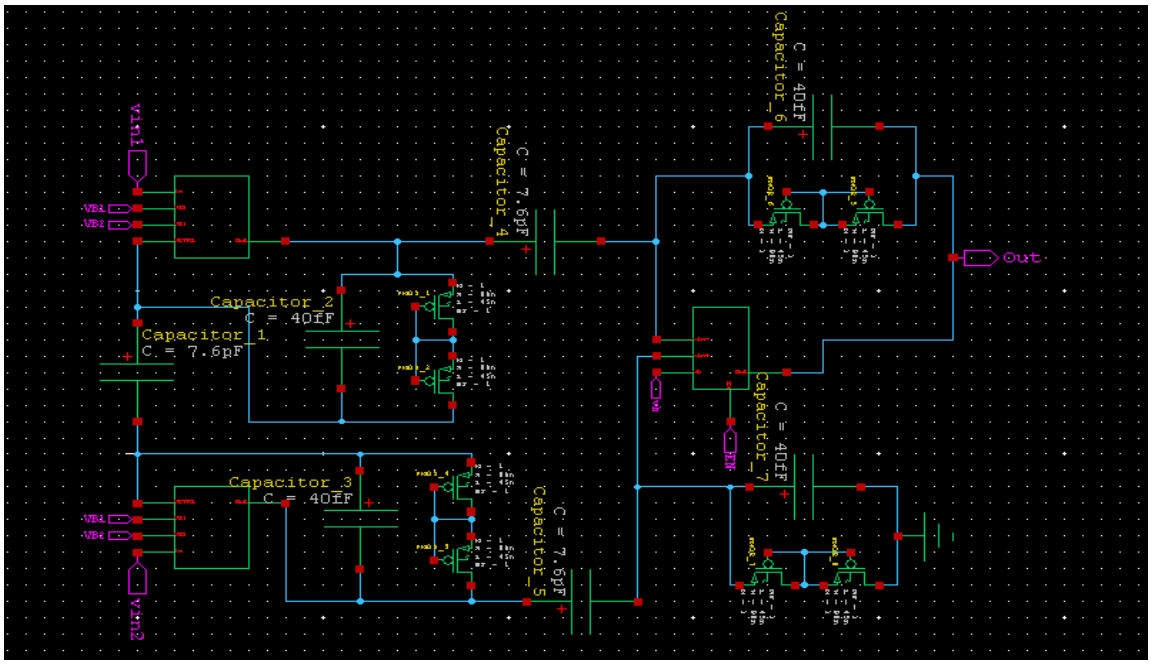

Figure.4.1 Schematic Of Proposed Instrumentational Amplifier

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SIMULATION:

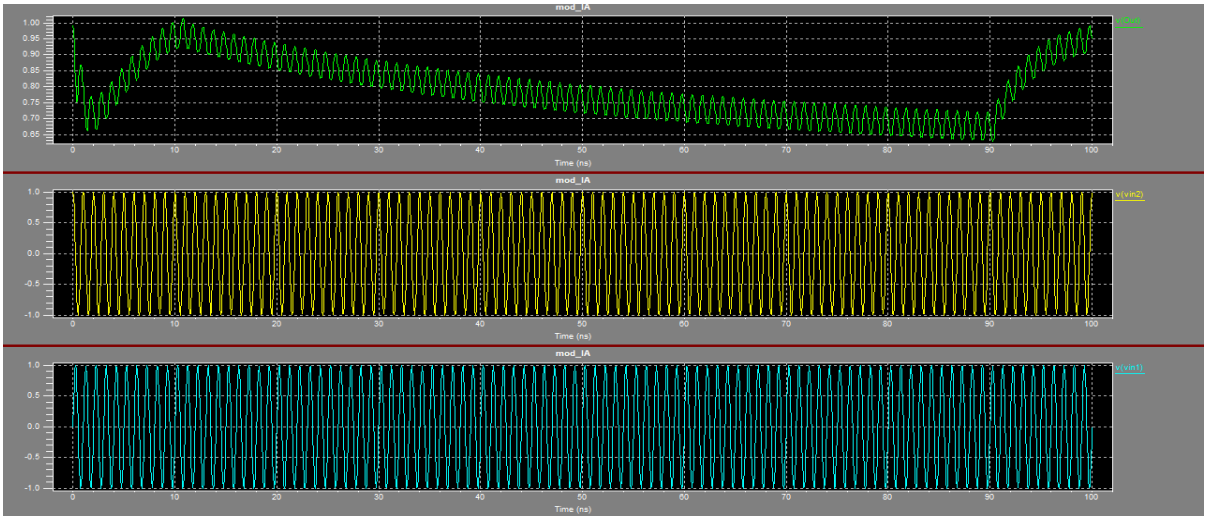

Figure.4.2 Waveforms For Proposed Instrumentational Amplifier

	Power	Delay	Transistor count
Conventional	50.73µ	0.5098ns	40
Proposed	50.10µ	0.47155ns	41

Figure.4.3 Comparison Table

V. CONCLUSION

The conclusion of the paper is that the proposed instrumentation amplifier (IA) design with a pseudo-differential inverter is able to achieve high common-mode rejection ratio (CMRR), also modified the two-stage operational amplifier structure using power gating header transistor and low input-referred noise for neural signal sensing applications.Here comparisons are drawn among conventional and proposed structures of Instrumentational amplifier for performance parameters such as power, transistor count and delay. All these schematic simulations are takes place in T-spice using tanner eda employing 45nm library files by performing transient analysis.

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