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Enhancing Efficiency of DC-DC Converter with Closed-Loop Control and Voltage Clamping Method for Reduced Switch Voltage Stress

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ABSTRACT: This research paper examines a proposed high-efficiency voltage-clamped DC-DC converter with reduced reverse recovery current and voltage stress. Conventional converters suffer from reverse-recovery problems in switching devices (diodes), leading to significant efficiency reduction and severe electromagnetic interference (EMI). Additionally, they face high voltage and current stress issues, resulting in high switching losses and poor conversion efficiency. The proposed converter is designed for a wide range of frequencies (5 KHz to 100 KHz) and implemented under open-loop and closed-loop conditions using MATLAB-SIMULINK. Simulation results are compared for both cases, demonstrating the closed-loop system's ability to maintain consistency. The converter's analysis is performed for a wide range of frequencies, input voltages, and duty ratios.

I.INTRODUCTION

In recent years, there has been an increasing demand for DC-DC converters with high voltage conversion ratios in various industrial applications, such as front-end stages for clean energy sources, DC backup energy systems for uninterruptible power supplies (UPS), high-intensity discharge (HID) lamps for automobile headlamps, and the telecommunication industry. Conventional boost converters cannot provide such high DC voltage ratios due to losses associated with the inductor, filter capacitor, main switch, and output diode. Even at extreme duty cycles, severe reverse-recovery problems arise, increasing the rating of the output diode and degrading conversion efficiency while causing severe electromagnetic interference (EMI). To improve conversion efficiency and voltage gain, numerous modified boost converter topologies have been investigated in the past decade. Many battery-powered applications require high-performance, high step-up DC-DC converters. For instance, in a HID lamp ballast used in automotive headlamps, where the start-up voltage can reach up to 400V, the DC-DC converter needs to boost the 12V battery voltage to 100V during steady-state operation. Another example is the front-end converter with dual inputs, where the 48V DC bus voltage needs to be boosted to about 380-400V for applications such as uninterruptible power supplies (UPS). The aim of this study is to design a high-efficiency voltage-clamped DC-DC converter with reduced reverse-recovery current and switch-voltage stress to provide a stable constant DC voltage. This is achieved through the manipulation of inductors and transformers to increase voltage gain and enhance the utility rate of the magnetic core. Voltage-clamped technology is used to reduce switch voltage stress and solve the reverse-recovery problem. Additionally, closed-loop control methodology can be utilized in the proposed converter to overcome the voltage-drift problem of the power source under varying load conditions. This project focuses on indirect DC/AC/DC converters utilizing an isolation transformer, which are widely used in applications such as battery chargers and dischargers, uninterruptible power systems, alternative energy systems, hybrid electric vehicles, and medical X-ray imaging. For applications where low input voltages need to be converted to high output voltages, current-fed converters are used, while for higher power applications, full-bridge boost converters are typically a good choice, which will be the focus of this project [1].

II.LITERATURE REVIEW

A critical assessment of the work has been done so far on high-efficiency voltage-clamped DC-DC converter with reduced reverse recovery current and voltage stress to show how the reverse recovery current and voltage stress has been reduced and how the converter efficiency improved. In [2] introduces a boost converter featuring an isolated active snubber to

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mitigate losses caused by the reverse-recovery characteristic of the boost rectifier and the turn-on discharge loss of the output capacitance of the boost switch. The proposed converter incorporates a coupled inductor, clamp capacitor, and ground-referenced n-type MOSFET within the active snubber configuration. Experimental evaluation conducted on a 1-kW, universal-line-range, boost input-current shaper confirms the effectiveness of the proposed converter. In [3] presented a novel family of DC-to-DC converters integrating clamping action, PWM modulation, and soft-switching (ZVS) in both active and passive switches. The proposed converters address limitations observed in clamped mode DC-to-DC converters and ensure favourable switching conditions across all switching devices by effectively absorbing parasitic reactance. Theoretical analysis, simulations, and experimental results obtained from a laboratory prototype rated at 1600 W validate the efficiency of the proposed converters. In explained [4] two alternatives for implementing isolated DC-DC converters operating with high output voltage and supplied by unregulated low input voltage, tailored for telecommunication satellite applications. The proposed topologies, suitable for traveling wave tube amplifier (TWTA) applications, offer low mass, volume, and high efficiency. Experimental results obtained from laboratory prototypes verify the operational characteristics and efficiency of the proposed structures, catering to an output power of 150W, total output voltage of 3.2 kV, and input voltage varying from 26 V to 44 V. In [5] explained a family of high-efficiency, high step-up DC–DC converters designed without isolation, addressing applications requiring high voltage gain. The proposed converters, utilizing diodes and coupled windings, achieve high efficiency by recycling leakage energy and alleviating the reverse-recovery problem of the output rectifier. Theoretical analysis, practical design, and experimental results validate the performance of the proposed converters, outperforming their active-clamp counterparts. In [6] presented an enhanced regenerative soft turn-on and turn-off snubber applied to a boost pulse width-modulated (PWM) converter. The proposed boost soft-single-switched (SSS) converter operates with soft switching in a PWM manner without high voltage and current stresses, achieved through the use of an auxiliary inductor magnetically coupled with the main inductor. Detailed simulation and experimental results confirm the validity and effectiveness of the proposed converter.

III.METHODOLOGY

3.1 OPEN LOOP SIMULATION OF HIGH EFFICIENCY VOLTAGE CLAMPED DC-DC CONVERTER:

The Fig.1. shows the simulation circuit schematic of an open-loop high step-up DC-DC converter. The circuit is powered by a DC voltage source on the left. It uses an auto-winding transformer to achieve a high step-up voltage ratio. The transformer has coupled inductors connected to its primary side. A MOSFET switch is used for controlling the power flow to the transformer. On the secondary side, there are rectifier diodes to convert the AC to DC. A capacitor is connected across the output to filter the rectified voltage. The circuit employs a voltage clamping technique to limit the switch voltage stress. Additional diodes and capacitors are used for clamping and energy recovery purposes. The "Continuous power out" block represents the output load. Other blocks like "Scope" and "Display" are used for monitoring and displaying simulation results.

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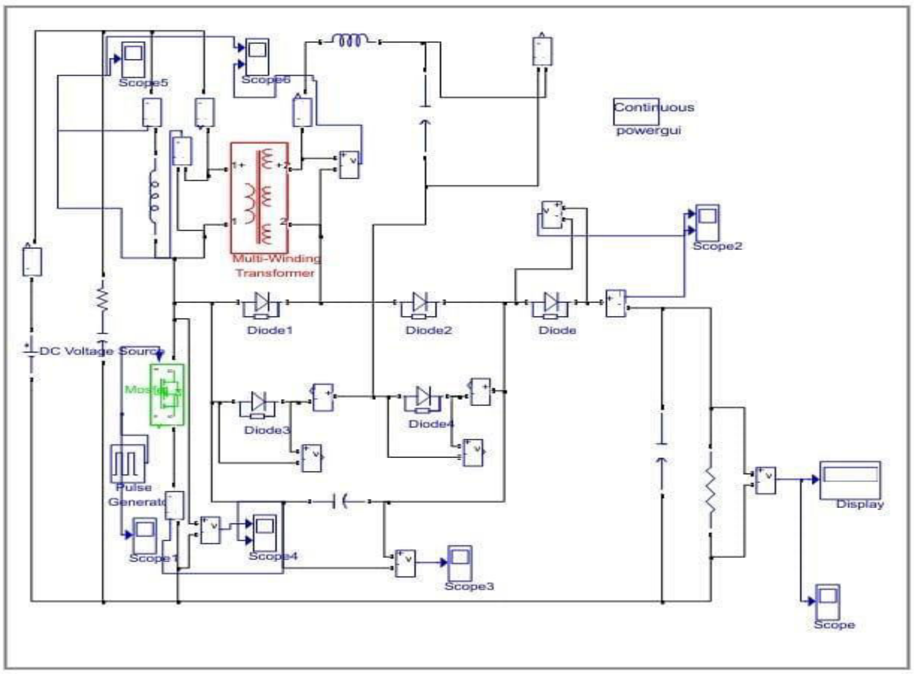

Fig.1 Open loop simulation of high efficiency voltage clamped DC-DC converter

In an open-loop implementation of this high efficiency voltage clamped DC-DC converter, there is no feedback control mechanism to regulate the output voltage. As a result, the key waveforms like output voltage, switch voltage, inductor currents etc. will exhibit different characteristics compared to the closed-loop operation:

Open Loop Waveforms Analysis: Output Voltage will vary significantly with input voltage changes and load variations. Poor regulation, with the output voltage drifting from the desired value over time. More ripples and fluctuations in the output voltage. The peak switch voltage stress will be higher without any clamping mechanism. More voltage spikes and ringing may be present across the switch. The inductor currents will have higher peak and RMS values without proper regulation. More ripples and imbalances in the currents due to lack of control. Diode reverse recovery currents may be higher due to uncontrolled di/dt.

3.2 Closed loop simulation of high efficiency voltage clamped DC-DC converter

The Fig 2. shows a simulation diagram or model for a closed-loop system, likely implemented in Simulink. It appears to be a power electronics or motor control circuit with various interconnected blocks representing different components and subsystems. The block labeled "Subsystem" which seems to be a critical part of the closed-loop control system. This subsystem is surrounded by other blocks representing different functional elements such as inverters, switches, transformers, and filters. closed-loop power electronics or motor control system, incorporating various subsystems and components necessary for regulating and controlling the output based on feedback signals and control algorithms implemented within the "Subsystem" block.

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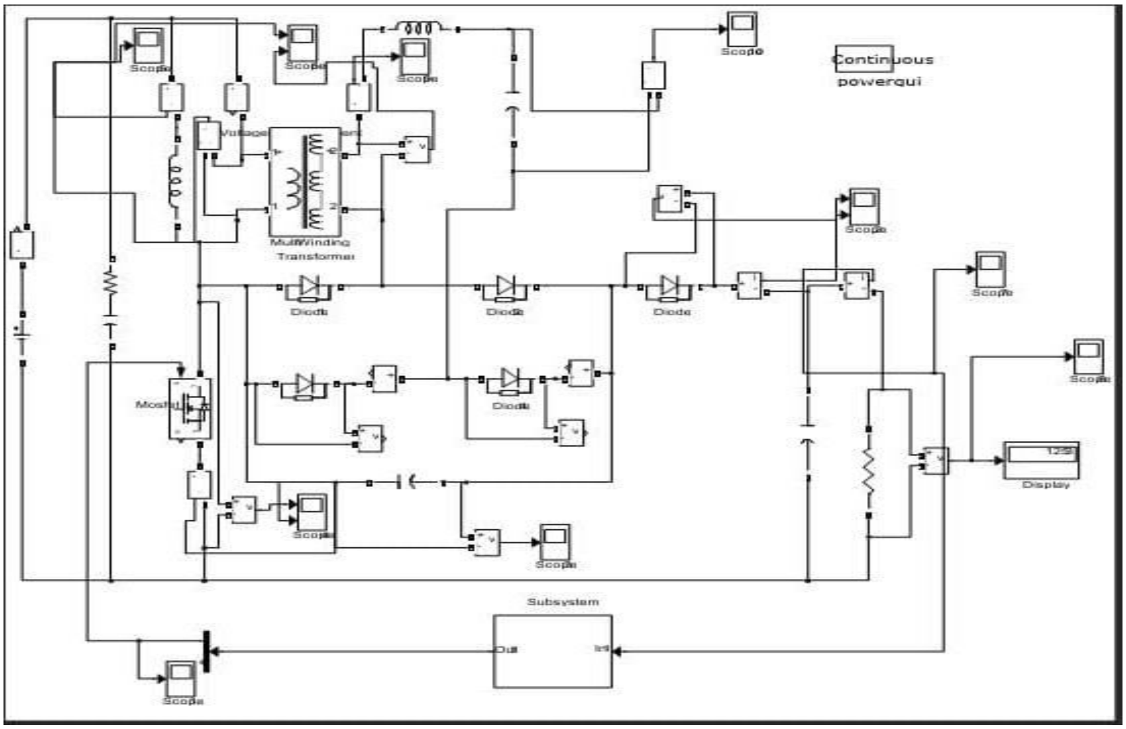

Fig.2. Closed loop simulation of high efficiency voltage clamped Dc-DC converter

Closed Loop Waveforms Analysis: The Closed Loop consists of Well-regulated Output voltage and maintained at the desired set value. Quick recovery from any transients caused by line/load disturbances. Low output voltage ripple. Switch Voltage: Peak switch voltage clamped to desired level by the voltage clamping circuit. Minimal voltage spikes due to controlled switching. Inductor Currents are Well-controlled with low ripple content and produces Balanced currents in multiple inductors. Diode Currents have a Controlled di/dt which minimizes reverse recovery currents. In summary, the closed-loop feedback control provides tight regulation over all waveforms, minimizing undesirable effects like voltage drift, current imbalances, switching losses etc. The open-loop waveforms will exhibit poor regulation characteristics.

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IV. RESULTS AND DISCUSSIONS

4.1 Open Loop Result:

The Fig 3. This waveform displays a periodic square wave pattern with sharp transitions between two voltage levels, approximately 0V and 25V. This pattern is characteristic of the switching behaviour of a power electronic device, such as a transistor or MOSFET, in a switch-mode power converter circuit. The square wave shape indicates that the switch is alternating between its on-state (conducting) and off-state (blocking) in a periodic manner, enabling the switching operation of the converter.

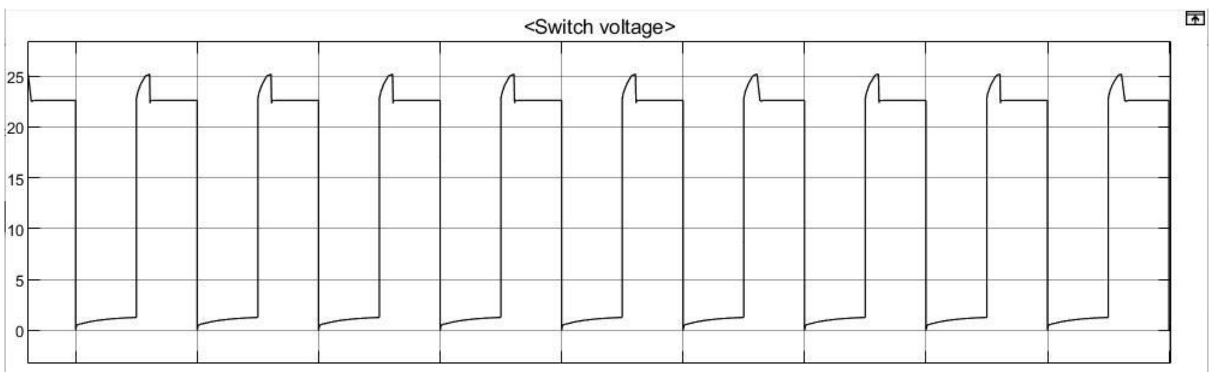

FIG 4.1.1: OPEN LOOP SWITCH VOLTAGE

The Fig. 4. This waveform exhibits a series of periodic current pulses with a peak amplitude of around 70A. These current pulses occur during the on-state (conduction period) of the switching device, indicating that current is flowing through the switch at those instances. The shape of the pulses suggests that the switch is operating in a hard-switching mode, where the current rises and falls rapidly during the switching transitions. The spacing between the pulses corresponds to the switching frequency of the converter, which can be determined from the time period between consecutive pulses. This waveform provides insights into the current conduction behaviour and switching characteristics of the power electronic switch within the converter circuit.

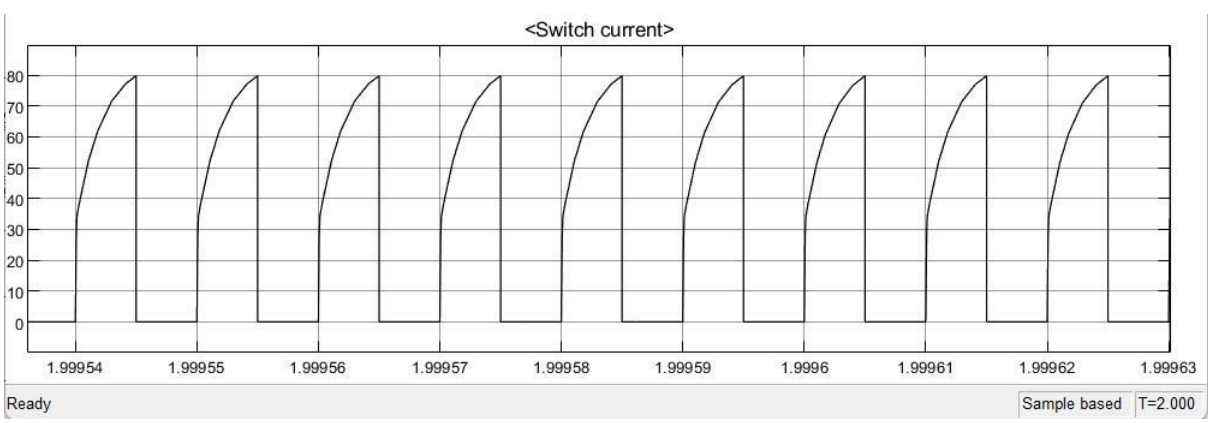

Fig. 4. Open loop switch current

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4.2 Closed Loop Result:

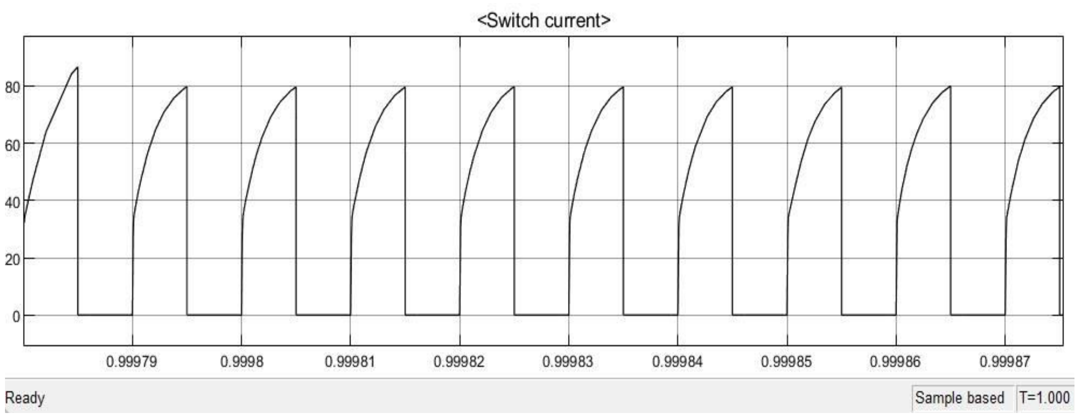

Fig. 5. Closed loop switch current

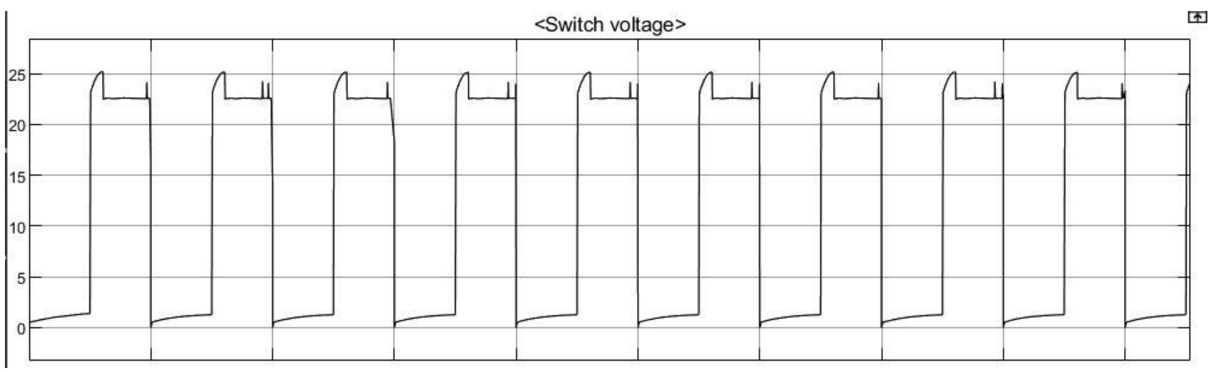

Fig. 6. Closed loop switch voltage

From Fig. 5 and Fig. 6. drawing a conclusion that the recovery current and voltage stress are reduced, and the closed-loop operation is increasing the efficiency of the converter, we need to analyze the provided waveforms and compare them with the expected behavior of a well-designed closed-loop converter.

1**. Recovery current reduction**: The switch current waveform shows a smooth, trapezoidal shape without any abrupt changes or spikes. This indicates that the recovery current, which typically manifests as a spike in the switch current during turn-off, is effectively minimized or suppressed. A reduced recovery current can lead to lower switching losses and improved efficiency.

2. **Voltage stress reduction**: The switch voltage waveform exhibits clean, rectangular pulses without any overshoots or ringing. This suggests that the voltage stress across the switch is well-controlled, and there are no significant voltage spikes or transients. Reduced voltage stress can improve the reliability and lifetime of the switching devices.

V.CONCLUSION AND FUTURE WORK

Based on the provided circuit diagrams and wave forms, which appear to represent open-loop and closed-loop simulations for a high-efficiency voltage-clamped DC-DC converter. The inclusion of both open-loop and closed-loop simulations allows for comprehensive analysis and evaluation of the converter's performance, efficiency, and behavior under different operating conditions. The voltage-clamped structure and the use of auxiliary components like diodes and capacitors aim to reduce recovery current and voltage stress, which could lead to improved efficiency and reliability compared to conventional converter designs. The detailed circuit diagrams and simulations provide a solid foundation for further theoretical analysis, design optimization, and experimental validation of the proposed converter topology.

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REFERENCES

[1] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-up switching-mode converter with high voltage gain using a switched- capacitor circuit," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, no. 8, pp. 1098–1102, Aug. 2003.

[2] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," *Proc. Inst. Elect. Eng.—Electr. Power Appl.*, vol. 151, no. 2, pp. 182–190,Mar. 2004.

[3] M. M. Jovanovic and Y. Jang, "A new soft-switched boost converter with isolated active snubber," *IEEE Trans. Ind. Appl.*, vol. 35, no. 2,pp. 496–502, Mar./Apr. 1999.

[4] E. S. da Silva, L. dos Reis Barbosa, J. B. Vieira, L. C. de Freitas, and J. Farias, "An improved boost PWM soft-single-switched converter with low voltage and current stresses," *IEEE Trans. Ind. Electron.*, vol. 48, no. 6, pp. 1174–1179, Dec. 2001.

[5] Q. Zhao and F. C. Lee, "High-efficiency, high step-up dc–dc converters,"*IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 65–73, Jan. 2003.

[6] M. D. Lukas, K. Y. Lee, and H. Ghezel-Ayagh, "Development of a stack simulation model for control study on direct reforming molten carbonate fuel cell power plant," *IEEE Trans. Energy Convers.*, vol. 14, no. 4, pp. 1651–1657, Dec. 1999.

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