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Data Retention Based Low Leakage Power TCAM For Network Packet Routing

C .Vijaya Bhaskar M.Tech(Ph.D), Rajesh.A, Rajitha.N, Sai Dhanush.C, Rajesh.G

Department of Electronics & Communication Engineering, Siddharth Institute of Engineering & Technology

Puttur, India

ABSTRACT: Recently there is a vast advancement in data transmission using wireless Communications. Content addressable memory (CAM) is one of the most promising hardware solutions for high-speed data searching and has many practical applications such internet protocol (IP) filters, and network switches. Since CAM stores the data in its internal memory elements and compares them with the search data in parallel, it can achieve much faster speed. The ternary content addressable memory (TCAM) is widely used in the routing table due to its high lookup performance. However, a large number of transistors would cause the power consumption of TCAM to be considerable. In this paper, a novel TCAM is proposed to reduce the leakage power dissipated in the memory

In this paper, a new state-preserved technique, named data retention based TCAM (DR-TCAM), is proposed to reduce the leakage power dissipated in the TCAM memory.

According to the continuous feature of mask data, the DR-TCAM can dynamically adapt the power source of mask cells so as to reduce the TCAM leakage power. Particularly, the mask data wouldn't be destroyed in the DRTCAM. The proposed TCAM structure was designed and implemented using 45nm technology in Tanner EDA tool.

I. INTRODUCTION

Mobile Communication plays a very important role in modern life. With the progress of telecommunication technology, a large number of applications are designed, such as video stream, on-line game, navigation, etc., and many of them demand low communication latency, high throughput, and high data rate. Consequently, rapid packet routing and data searching are two fundamental requirements for 4G/5G network routers. Ternary content addressable memory (TCAM) has the feature of fast and parallel data searches. The routing table implemented with TCAM can easily achieve the goal of rapid routing. However, this attractive feature would induce considerable leakage power since a large number of transistors are used.

For reducing TCAM leakage (static) power consumption, many techniques had been proposed in the past decade [1-5]. Some of them reduce leakage power by optimizing SRAM structure [1], using dual-voltage architecture [2], and using dynamic power source [3]. All of these methods effectively reduce the power consumption of TCAM; however, most of them would destroy the data when the power supply or data signals are gated. External storages or control signals are

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Y.-J. Chang is with the Department of Computer Science and Engineering, National Chung Hsing University, Taichung 407, Taiwan.

K.-L. Tsai is with the Department of Electrical Engineering, and Research

required when the destroyed data need to be recovered. This implies that the TCAM would consume much power and spend much time to recover these data.

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In this paper, a novel TCAM architecture with data retention technique, named data retention based TCAM (DR-TCAM), is proposed to reduce the leakage power consumption of TCAM. In our design, each TCAM entry is partitioned into several segments. In each segment, the power source of internal mask cells drives from the most significant bit (MSB) and least significant bit (LSB) cells, respectively. Due to the continuous feature of mask data, except for the boundary segment, all segments would be inactivated to minimize the leakage power consumption. Unlike the previous works [3-5], in DR-TCAM the mask data are still preserved in low-leakage mode, i.e., neither external control nor TCAM rewriting behavior is needed when mask data need to be restored. A 1024 32 TCAM was implemented with TSMC 40nm technology to verify the DR-TCAM design. The experimental results show that compared to the traditional design the DR-TCAM can reduce 41% leakage power with only 1.1% search performance loss.

The rest of this paper is organized as follows. Section II introduces the TCAM architecture and investigates the related works. Section III describes the proposed DR-TCAM architecture in detail. The experimental results are shown in Section IV. Finally, Section V provides a brief conclusion.

II.PRELIMINARY AND RELATED WORKS

A.Traditional TCAM Architecture

As shown in Fig. 1, a TCAM cell is composed of three parts, i.e., XOR-type CAM cell, evaluation logic, and SRAM cell. The XOR-type CAM cell stores the data (D) that would be compared with the search data (SL and SL). The SRAM cell stores the mask data (M) to indicate whether this TCAM cell is in don't-care state (i.e., "X" state) or not. When the TCAM cell is in the "X" state, the compare result must be matched.

The function of the network router is forwarding the input packets to other routers according to the destination IP address of the packet header. The mask (prefix) bit is used to determine the domain of IPv4 (IPv6) address. TABLE I shows the examples of IPv4 address mask and the corresponding domain address. A TCAM entry stores the IP data in the CAM cells and

Center for Smart Sustainable Circular Economy , Tunghai University, Taichung 407, Taiwan (R.O.C) (e-mail: kltsai@thu.edu.tw).

Y.-C. Cheng is with the Department of Computer Science and Engineering, National Chung Hsing University, Taichung 407, Taiwan.

Corresponding author: K.-L Tsai.

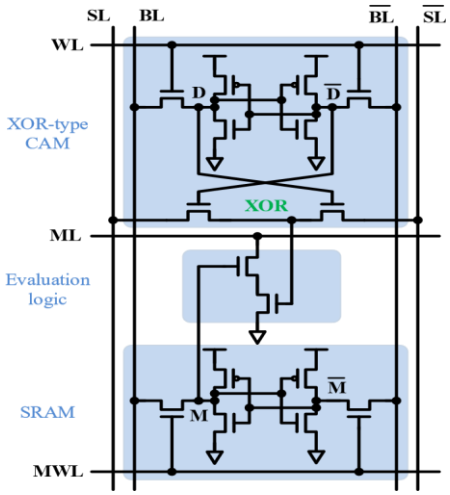

Fig. 1. One traditional TCAM cell is composed of XOR-type CAM cell, evaluation logic, and SRAM cell.

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TABLEI
EXAMPLES OF IPADDRESS PREFIX AND DOMAIN ADDRESS

Mask/Prefix	IP address / Mask data	
140.120.7.14/24 Care bits: 24 Don't Care bits: 8	IP	10001100.01111000.00000111.00001110
	Mask	11111111.11111111.11111111.00000000
	Domain	10001100.01111000.00000111.00000000
140.120.3.45/27 Care bits: 27 Don't Care bits: 5	IP	10001100.01111000.00000011.00100101
	Mask	11111111.11111111.11111111.11100000
	Domain	10001100.01111000.00000011.00100000

the mask data in the SRAM cells. For example, 140.120.7.14/24 can be divided into two parts. The IP 140.120.7.14 is stored in the CAM cells. The mask length is 24 which is stored in the SRAM cells as 255.255.255.0, i.e., 11111111.11111111. 11111111.00000000. The domain of this IP address can be calculated by using logical AND, and the result is 10001100.01111000.00000111.00000000, i.e., 140.120.7.0. The number 24 represents that there are 24 care bits and 8 don'tcare bits in this IP. As shown in TABLE I, it is obvious that the mask data consists of continuous 1s and 0s.

B.Related Works

Because our design aims to reduce the TCAM static power consumption, we only survey the related works on the same issue. Mohan and Sachdev [1] presented a 5T SRAM to eliminate one of the subthreshold leakage paths. Chen et al. [2] designed a dual-voltage architecture to lower the supply voltage of major searching components so that the leakage power can be reduced when the major searching components are temporal unused. According to the state of mask data, Chang [3] proposed the dynamic power source (DPS) technique to reduce the leakage currents of TCAM. When the mask cell is in care state, the TCAM cell work as normal; however, when the mask cell is in "X" state, the DPS technique would block the supply voltage of corresponding CAM cell and destroy the redundant

TABLEII
THE THREE KINDS OF TCAMSEGMENTS FOR IPV4

Mask Data segment	**Meaning**	**Example in Fig. 2**
1…1…1	All 1s	S1 and S2
1…10…0	Boundary segment	S3
0…0…0	All 0s	S4

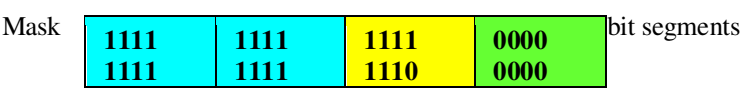

Fig. 2. An example of 4-segment mask data 255.255.254.0

data so as to suppress the leakage currents of CAM cell. Different from the traditional power gating technique, no extra transistor was needed for the DPS-based TCAM.

Based on the continuous features of mask data, Chang et al. [4] further introduced a two-side self-gating (TSSG) scheme and also implemented the mask vertical control (MVC) scheme [5] for reducing the leakage power consumption of TCAM. In [4], a TSSG-based TCAM entry is divided into several segments, and when the mask data of one segment are the same, the TSSG-based TCAM cut off unnecessary charge and discharge paths in SRAM cells.

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The MVC technique also turns off the unnecessary power supplies of CAM cells and SRAM cells depending on the top mask data of a segment. When the top mask data is in the "X" state, all CAM and SRAM cells are power gated to reduce the leakage power, on the contrary, when the top TCAM cell is in the care state, the TCAM cells work as normal.

Note that these designs destroy those temporal unused data. More power and time are required when the destroyed data need to recover. Instead, our design, i.e., DR-TCAM, would reduce leakage power consumption as well as preserve the mask data.

III.DATA RETENTION BASED TCAM(DR-TCAM)

A.Mask Data Segment

The main idea of the DR-TCAM is using the feature of continuous 1s and 0s of mask data to minimize the static power consumption of TCAM. First, an N-bit TCAM entry is partitioned into S segments, and each segment has L bits data. TABLE II shows the three kinds of mask segments, i.e., all 1s, all 0s, and boundary segments. The corresponding example is shown in Fig. 2. The 32-bit mask data 255.255.254.0 is partitioned into 4 segments (S1 to S4), and each segment has 8 bits. The first two segments (S1 and S2) are the case of all 1s. The segment S3 is the boundary segment and the segment S4 is the case of all 0s.

According to the continuous feature, the segment type can be determined by checking the MSB and LSB of a segment. As shown in TABLE II, when the LSB is 1, this segment must be all 1s segment; when the MSB is 0, this segment must be all 0s segment; otherwise, the segment is called the boundary segment. B.Data Retention

Fig. 3 shows one DR-TCAM segment, in which two inverters, i.e., INV_M and INV_L, are inserted to provide VDD

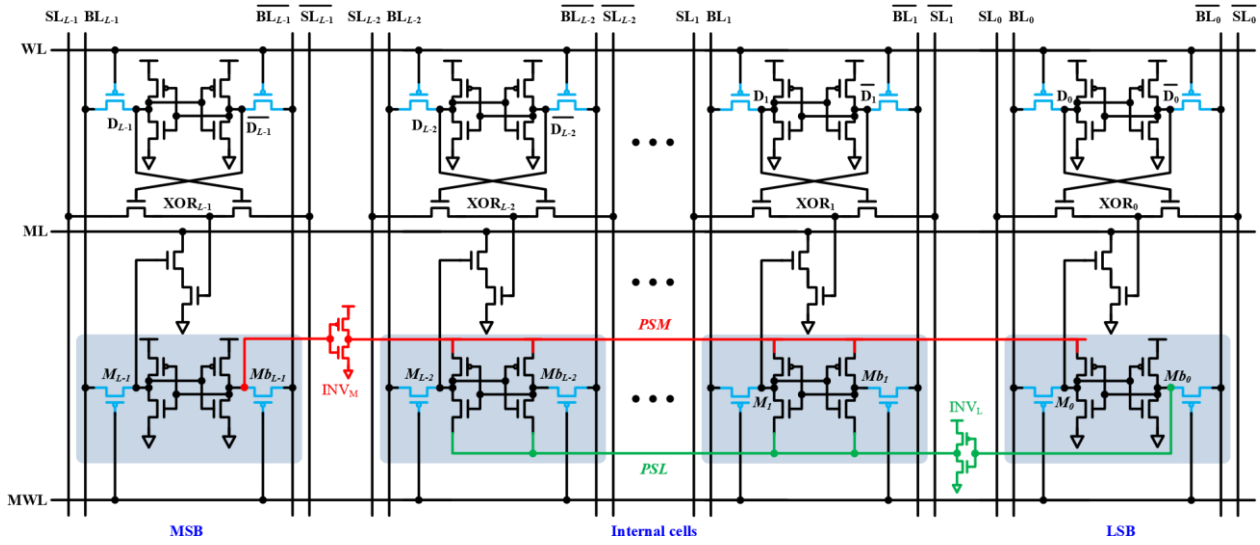

Fig. 3. The proposed low leakage TCAM design with data retention technique.

(charge) path and GND (discharge) path for the SRAM cells. The VDD of internal mask cells comes from the MSB cell, and the GND of internal mask cells comes from the LSB cell. Note that the VDD of left-side inverter of the LSB cell is also connected with PSM to lower the leakage currents of the LSB cell in all 0s segment.

Since the leakage current of NMOS is larger than that of PMOS with the same feature size [6]. To further reduce the leakage power consumption, instead of using NMOS, the pass transistors of CAM and SRAM cells are replaced by PMOSs, which is also shown in Fig. 3.

Take Fig. 2 for example, the 32-bit TCAM entry is partitioned into 4 segments, each segment has 8 TCAM cells (L = 8, N = 32, and S = 4).

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1) Segments S1 and S2 (all 1s segment): In the all 1s segment, the PSM and PSL are both H so that the VDD paths and GND paths of internal SRAM cells are both set to VDD. This makes the internal cells' data M_6 to M_1 remaining 1, but the inverse data Mb_6 to Mb_1 are raised from 0 to 1 , as shown in Fig. 4(b). Because the voltage difference between VDD and GND path of the internal mask cells is minimized, the leakage power can be largely reduced.
2) Segment S4 (all 0s segment): In the all 0s segment, the VDD and GND paths of internal SRAM cells are both set to GND. This makes the internal cells' data M_6 to M_1 still remaining 0, but the inverse data Mb_6 to Mb_1 are discharged from 1 to 0 , as shown in Fig. 4(c). Similarly, the leakage power consumption can be largely reduced.
3) Segment S3 (boundary segment): In the boundary segment, the MSB M_7 must be 1 and the LSB M_0 must be 0. Accordingly, the PSM and PSL are set to VDD and GND, such that the internal SRAM cells work as normal. No leakage power can be saved in this case.

C.SRAM Cell Leakage Currents Analysis

To illustrate the DR-TCAM effect on leakage power reduction, Fig. 4 shows the SRAM leakage current paths of different segment types, in which the red solid lines represent the subthreshold leakage current I_{sub} of NMOS and the red

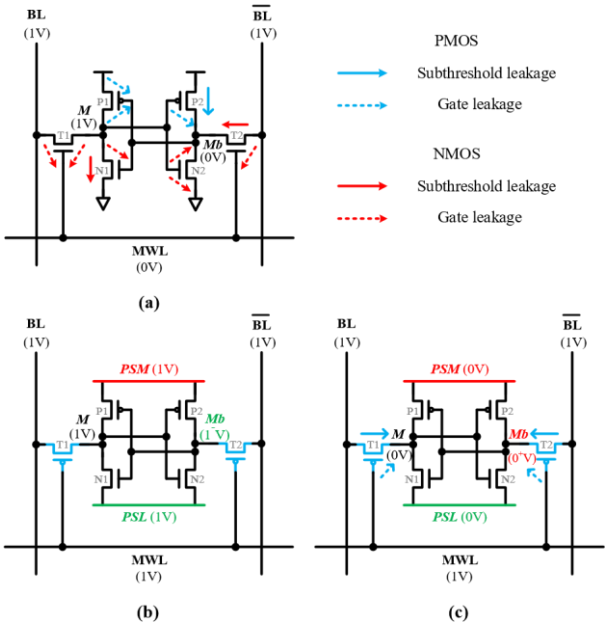

Fig. 4. Leakage current paths of (a) the traditional SRAM, (b) the DR-TCAM internal mask cell in all 1s segment, and (c) the DR-TCAM internal mask cell in all 0s segment. dotted lines represent the gate leakage current I_{gate} of NMOS. The blue solid and dotted lines represent Isub and Igate of PMOS, respectively. The detailed leakage power estimated by HSPICE with TSMC 40nm technology are summarized in TABLE III.

Fig. 4(b) shows the leakage current paths of the DR-TCAM internal mask cell when the segment is all 1s segment. From Fig. 4(b) and Table III, it is clear that in this case, the internal mask cell consumes very little leakage power for the reason that the voltage difference between 1V and 1 V can be ignored. Therefore, compared to the traditional SRAM cell, the leakage power saving of DR-TCAM's internal mask in all 1s segment is about 99%.

Fig. 4(c) shows the leakage current paths of the DR-TCAM internal mask cell when the segment is all 0s segment. In Fig.

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TABLEIII
LEAKAGE POWER OF MASK CELL IN ALL 1S AND 0S SEGMENT

SRAM (single cell)	Leakage Power (Watt)		Reduction Percentage	
	all 1s seg.	all 0s seg.	all 1s seg.	all 0s seg.
(a) Traditional SRAM	2.060e-08	2.060e-08	-	-
(b) DR-TCAM Internal SRAM	1.454e-10	5.973e-09	99.29%	71.00%
(c) DR-TCAM LSB SRAM	1.681e-08	1.592e-08	18.40%	22.72%

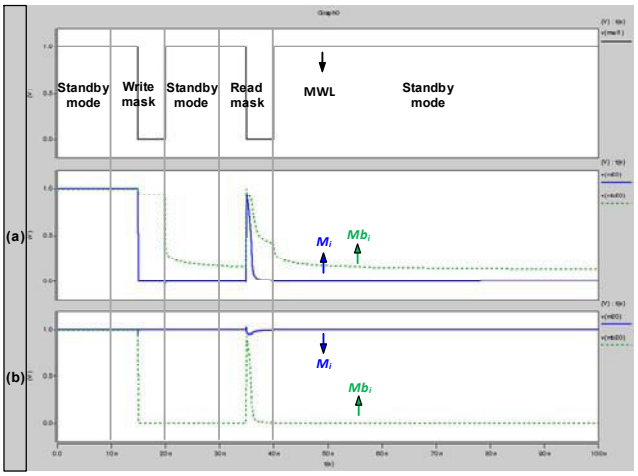

Fig. 5. The correct waveforms for all 1s segment being written and changed into (a) all 0s segment, and (b) boundary segment.

4(c), the leakage currents of transistors P1, P2, N1, and N2 can be minimized because the sources and drains of these transistors are all set in 0V. However, the I_{sub} of T2 would increase compared with the traditional design, and cancel out a little leakage power saving from other transistors. As shown in Table III, the leakage power saving achieves 71% for the internal mask cell in all 0s segment.

IV.EXPERIMENTAL RESULTS

In this paper, all TCAM designs are implemented with TSMC 40nm technology and simulated with HSPICE in 25˚C and 1.0V power supply. The TCAM size is 1024 32, which means that there are 1024 entries, and each entry is 32-bit.

A.Functionality of DR-TCAM

To verify the DR-TCAM write and read function in standby (low-leakage) mode, we first write the mask data, and then read them after 10ns. Fig. 5 shows the case of all 1s segment. From Fig. 5(a), it is clear that an all 1s segment can be written and changed into all 0s segment successfully, and then the data can be read correctly. Besides writing all 0s,

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the DR-TCAM can also perform the successful write from all 1s segment to the boundary segment, as shown in Fig. 5(b). Similarly, Fig. 6 shows the correct waveforms for all 0s segment being written and changed into all 1s segment and boundary segment, respectively. Therefore, the functionality of DR-TCAM design is verified and works well while reducing leakage power consumption.

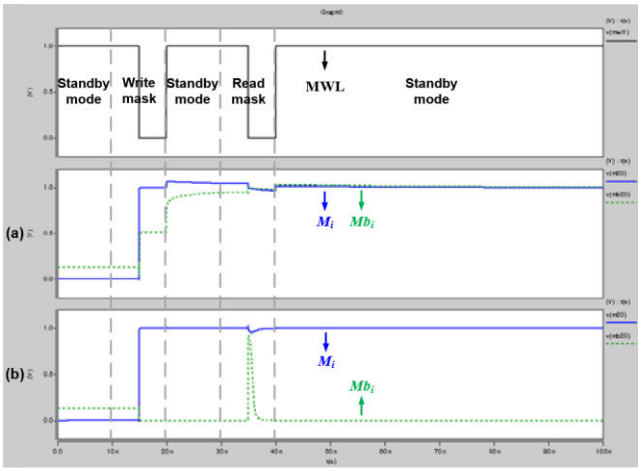

Fig. 6. The correct waveforms for all 0s segment being written and changed into (a) all 1s segment, and (b) boundary segment.

B.Leakage and Total Power Reduction

For a real data distribution, three routing table benchmarks from BGP Report [7], including AS1221, EQIX, and APNIC, are used to examine all TCAM designs. To highlight the superiority of DR-TCAM in leakage power reduction, besides the traditional TCAM design, three low-leakage designs,

including DPS-TCAM [3], TSSG-TCAM [4], and MVC-

TCAM [5], are also implemented and simulated with the same condition for comparison. Note that for a fair comparison, the

best case of each TCAM is selected, i.e., DPS_{GND} for DPSTCAM [3], 8(24) partition for TSSG-TCAM [4], and MVC_Seg32 for MVC-TCAM [5]. In our previous evaluation, DR-TCAM demonstrates the best result when segment size is 8-bit (Seg8). Thus, the best configuration of DR-TCAM is Seg8.

TABLE IV shows the detailed results, including the leakage power consumption and total power consumption of each TCAM. The average power reduction is further illustrated in Fig. 7, from which all TCAM designs can effectively reduce the leakage power consumption compared to the traditional TCAM. Among them, the DR-TCAM and TSSG-TCAM reduce much leakage power than the others, i.e., 41% and 30%, since the continuous feature of mask data is utilized in both of these two TCAM designs.

For total power consumption, the TSSG-TCAM and the DRTCAM can save 7% to 12% total power, but the DPS-TCAM and the MVC-TCAM consume much more total power than the traditional TCAM. In TABLE IV, all TCAM architectures are designed for the goal of low leakage power consumption; however, the total power consumption is composed of dynamic power and leakage power. Both the DPS-TCAM and the MVCTCAM use the search-enable scheme and need additional pulldown NMOS transistors between the evaluation logic and the GND so as to prevent short-circuit current. Unfortunately, these additional pull-down NMOS transistors increase the capacitance of MLs twice than that of the traditional TCAM. That is to say that the search-enable scheme reduces SLs' power consumption

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but increases the MLs power consumption, and causes the total power consumption of the DPS-TCAM and the MVC-TCAM higher than the traditional TCAM.

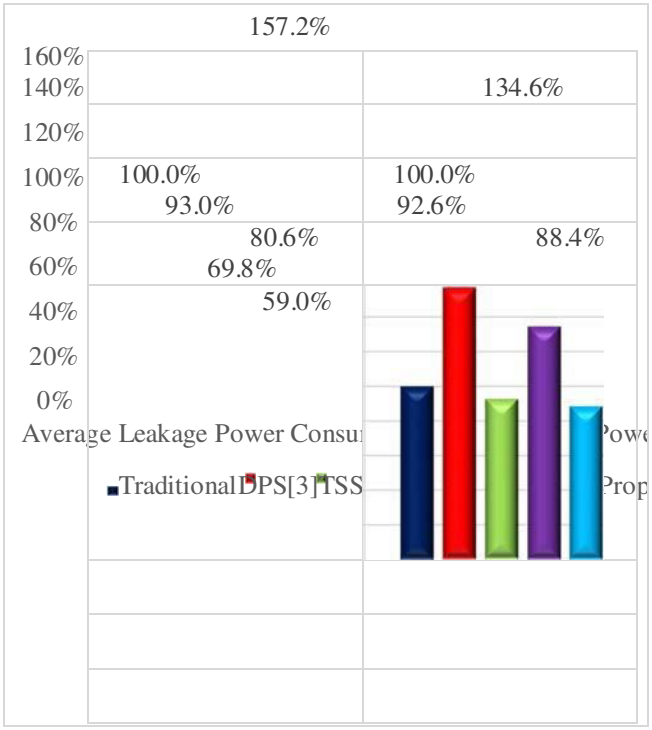

Fig. 7. Average power reduction for all TCAM designs.

TABLEIV
THE POWER CONSUMPTION OF LOW LEAKAGE TCAMDESIGNS

Architecture \ Benchmark		*AS1221*		*EQIX*		*APNIC*	
		Power Consumption (Watt)	Reduction Percentage	Power Consumption (Watt)	Reduction Percentage	Power Consumption (Watt)	Reduction Percentage
Traditional TCAM	Leakage Power	1.401e-03		1.398e-03		1.398e-03	
	Total Power	5.749e-03		5.311e-03		5.300e-03	
DPS-TCAM [3]	Leakage Power	1.375e-03	1.86%	1.263e-03	9.66%	1.265e-03	9.51%
	Total Power	8.801e-03	-53.09%	8.476e-03	-59.59%	8.432e-03	-59.09%
TSSG-TCAM [4]	Leakage Power	9.311e-04	33.54%	9.998e-04	28.48%	9.992e-04	28.53%
	Total Power	5.297e-03	7.86%	4.950e-03	6.80%	4.907e-03	7.42%
MVC-TCAM [5]	Leakage Power	1.237e-03	11.71%	1.074e-03	23.18%	1.072e-03	23.32%
	Total Power	7.613e-03	-32.42%	7.268e-03	-36.85%	7.143e-03	-34.77%
Proposed DR-TCAM	Leakage Power	8.123e-04	**42.02%**	8.331e-04	**40.41%**	8.308e-04	**40.57%**
	Total Power	5.114e-03	**11.05%**	4.677e-03	**11.94%**	4.677e-03	**11.75%**

C.Search Performance

TABLE V shows the search latency of different TCAM designs. Compared to the traditional TCAM, the search overhead of the TSSG-TCAM is 2.03% and the search overhead of the DR-TCAM is 1.11%. Both of the DR-TCAM and TSSG-TCAM have performance penalties less than 2.50%, since the evaluation logics of these two TCAMs are

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the same as the traditional TCAM. However, the search-enable scheme discharges much MLs' capacitances than the traditional TCAM, and results in longer search latency.

V.CONCLUSION AND FUTURE STUDIES

In this paper, we propose a low leakage TCAM design, called DR-TCAM. By using the continuous feature of mask data, the DR-TCAM can minimize the voltage difference between VDD and GND of internal mask cells so as to minimize the leakage power consumption. Unlike the previous TCAM designs, in the DR-TCAM all data can be preserved even in the standby mode. The simulation results show that the DR-TCAM outperforms the related techniques in power reduction and search performance. Compared to the traditional design the DR-

TABLEV
THE SEARCH LATENCY OF DIFFERENT TCAMDESIGNS

Architecture	Latency (ps)	Overhead
Traditional TCAM	79.39	-
DPS-TCAM [3]	83.83	5.59%
TSSG-TCAM [4]	81.00	2.03%
MVC-TCAM [5]	84.27	6.15%
DR-TCAM	80.27	1.11%

TCAM can reduce 41% leakage power with only 1.1% search performance loss.

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