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Dual Distribution Static Compensator with Neutral Capacitor for TPFW Distribution System

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ABSTRACT:This paper proposes a dual three leg single dc link capacitor based DSTATCOM. It is used for the compensation purpose in three phase four-wire distribution systems. In this topology, the inverter1 is connected to the line through filter1 and the inverter2 is connected to the line through filter2. This topology uses two three-leg inverters. The dc link is provided as common to both the inverters by means of single dc link capacitor. At the same time in order to compensate the neutral current, the small ac capacitor is connected between negative of the dc link capacitor and the ground. The control algorithm used in this topology has to compensate the unbalanced source current and neutral current by making them as balanced sinusoidal one. The unbalance in the source currents is due to three phase linear unbalanced load and non-linear load. The control algorithm also have the ability to share the reactive powers between the two VSIs used in the dual DSTATCOM topology. Simulation studies for the topology is carried out and its results are presented.

KEYWORDS:Distribution Static Compensator (DSTATCOM), Voltage Source Inverter (VSI), Instantaneous Symmetrical Component Theory (ISCT), Hysteresis Band Current Controller (HBCC), Proportional Integral (PI) Controller

I. INTRODUCTION

Normally, the DSTATCOMs are used for the purpose of load compensation, harmonic elimination and power factor corrections. It is normally a power quality device used for improving the waveform quality of currents in the systems using unbalanced loads and non-linear loads. It is given briefly in [1,2]. For high power applications, the usage of DSTATCOM gets limited because of their high current ratings of their inverter switches and its switching characteristics. So in high power applications parallel operation of more low power DSTATCOMs are used for compensation purpose. It is explained in [3,4]. The detailed explanation of using parallel active power filters are given in [5]. It shows the parallel operation of high and low frequency active power filters (APF). The system is coupled to the line through L and C filters. Each APF is connected to line by different L,C networks, which helps the system to eliminate the respective harmonic orders. The main drawback of these kind of parallel active power filter topology is that it cannot be able to compensate the neutral current present in the system. Hence it can suitable for three phase three-wire distribution systems only. But in case of three phase four-wire distribution systems, there always exists the neutral current as a result of using unbalanced load. It must be compensated to eliminate the overload stress on the neutral conductor. There are different types of VSI topologies available for compensation purpose. It is explained in [6,7,8]. From the available DSTATCOM topologies, split capacitor based DSTATCOM topology has less number of VSI switches. It also has the capability to control its VSI switches independently. The above discussed parallel inverter scheme is used in unified power quality conditioner (UPQC) and its applications. It is mentioned briefly in [9]. But all of these VSI topologies are affected by voltage unbalance issue across their dc link capacitors. It results in unequal voltage stress across their VSI switches which in degrades the compensation performance of the system. The split capacitor based DSTATCOM topologies are explained in [10,11]. Many control schemes are designed to avoid the voltage unbalancing issue across the dc link capacitors in split capacitor based DSTATCOM topology. It is given briefly in [10,11].

In this paper, a dual DSTATCOM topology is introduced for compensating three phase four-wire distribution systems. This topology has two VSIs (Inv1 and Inv2). Both the VSIs shares the common dc link through single dc link capacitor which is connected between the two VSIs. In order to compensate the neutral current, a small ac capacitor is connected between negative terminal of dc link capacitor and ground. The advantage of this topology are less voltage

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unbalancing issue and the amount of dc component in the system is less when compared to the split capacitor based DSTATCOM topology. It also has the advantage of using reduced ratings of VSI switches and dc link capacitor when compared to single dc link capacitor based DSTATCOM. There are two control techniques used in this topology. One is instantaneous symmetrical component theory (ISCT) [14] to generate the reference filter currents for both the VSIs. Another control technique is hysteresis band current controller (HBCC) [8] to generate the pulses or firing signals for the switches of both the VSIs.

II. PROPOSED DUAL VSI TOPOLOGY OF DSTATCOM

Fig 1 represents the dual VSI topology of DSTATCOM. In this topology, three leg VSIs are used. It is named as Inv1 and Inv2. Both the VSIs shares the common dc link with single dc link capacitor as C_{dc}. To provide unbalance in the system linear unbalanced load and non-linear load is connected to the system. This topology also contains the feeder resistance and inductance as R_f and L_f. The neutral capacitor connected between the bottom of the VSIs and ground is denoted as C_n. The three phase compensation currents provided by Inv_1 is denoted as i_{fa1}, i_{fb1}, i_{fc1} and the three phase compensation currents provided by Inv2 is denoted as i_{fa2}, i_{fb2}, if_{c2}. The three phase source currents are represented as i_{sa}, i_{sb}, i_{sc}. The three phase load currents are represented as i_{la}, i_{lb}, i_{lc}. Three phase source voltages are represented as V_{sa}, V_{sb}, V_{sc}. Three phase fundamental positive sequence voltages are represented as v_{ta}, v_{tb}, v_{tc}.

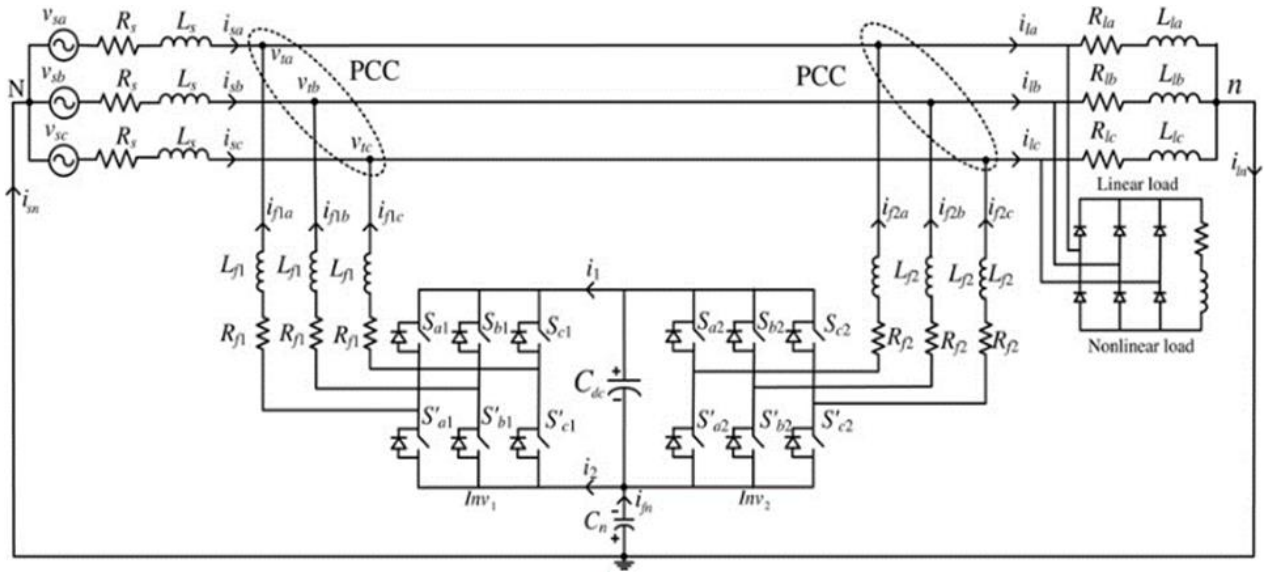

Fig. 1:Proposed dual VSI topology of DSTATCOM

III. DESIGN OF DC LINK CAPACITOR AND NEUTRAL CAPACITOR

(i) Design of DC link capacitor (C_{dc})

The main aim of the dc link capacitor is to provide dc voltage with minimum ripples to energize the VSIs connected with it. It also have the capacity to supply reactive as well as

harmonic power of the load. The energy balance equation of the dc link capacitor is given by the equation,

$$\Delta E = \left(2X - {}^{X}/_{2}\right) nT \qquad (1)$$

Where X is the KVA of the system. The assumption is made that the DSTATCOM is working with half (X/2) twice (2X) KVA handling capacity for n cycles. T is the time period of voltage or current waveform.

The dc capacitor voltage can be allowed to vary between the values of $3.4V_m$ to $3.0V_m$. By using the equation (1)

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$$\frac{1}{2}C_{dc}[(3.4V_m)^2 - (3.0V_m)^2] = \left(2X - {}^{X}/_{2}\right) nT \quad (2)$$

$$C_{dc} = \frac{2\left(2X - {}^{X}/_{2}\right) nT}{(3.4V_m)^2 - (3.0V_m)^2} \quad (3)$$

(ii) Design of neutral capacitor (C_n)

The neutral current to be compensated must be known to design the value of neutral capacitor. In order to design the neutral capacitor, the imaginary parts of 'a' phase Inv_1 current is equated to the 'a' phase load current. The 'a' phase filter current of Inv_1 is given as,

$$I_{fla} = \frac{V_1 - V_{ta1}}{R_{f1} + j(X_{f1} - \left(\frac{X_{cn}}{\alpha}\right))} \quad (4)$$

Where V_1 is given by,

$$V_1 = \frac{m_a V_{dc}}{\sqrt{2}} = \frac{V_{dc}}{2\sqrt{2}} \quad (5)$$

m_a represents the amplitude modulation index. In the analysis, its value is taken as 0.5.

The phase 'a' load current of Inv_1 is given as,

$$I_{la1} = \frac{\alpha V_{ta1}}{R_{la} + jX_{la}} (6)$$

Equating the imaginary parts of equation (4) and (6), we get

$$\frac{\alpha V_{ta1} X_{la}}{R_{la}^2 + X_{la}^2} = \frac{V_1 - V_{ta1}}{R_{f1}^2 + (R_{f1}^2 + (X_{f1} - \left(\frac{X_{cn}}{\alpha}\right))^2} \left(X_{f1} - \frac{X_{cn}}{\alpha}\right) \quad (7)$$

In order to find out the value of C_n, the equation (7) must be solved by substituting the known values in it so that the value of X_{cn} can be calculated. From X_{cn}, we can able to find out the value of C_n.

IV. CONTROL ALGORITHM

The steps to be followed are,

(i) Generate the reference filter currents (i^*_{fabc}).

(ii) Compare the reference filter currents (i^*_{fabc}) with the actual filter currents (i_{fabc}) and generate the pulses for VSI switches.

(iii) Maintain the dc link voltage (V_{dc}) at a reference value (V_{dcref}) with the help of PI controllers.

Step 1: Generate reference filter currents (i^*_{fabc})

It is generated by using Instantaneous Symmetrical Component Theory (ISCT). Since the source voltages are being distorted due to the presence of feeder impedance on the line, it cannot be used for the generation of reference currents. Hence the ISCT are built by using the sinusoidal fundamental positive sequence components of the distorted three phase source voltages. It is given as,

$$i^*_{fa} = i_{la} - \left(\frac{v^*_{ta1} + \beta\,(v^*_{tb1} - v^*_{tc1})P_1}{\sum_{j=a,b,c} v^{+2}_{tj1}}\right)$$

$$i^*_{fb} = i_{lb} - \left(\frac{v^*_{tb1} + \beta\,(v^*_{tc1} - v^*_{ta1})P_1}{\sum_{j=a,b,c} v^{+2}_{tj1}}\right)$$

$$i^*_{fc} = i_{lc} - \left(\frac{v^*_{tc1} + \beta\,(v^*_{ta1} - v^*_{tb1})P_1}{\sum_{j=a,b,c} v^{+2}_{tj1}}\right) (8)$$

Where, (i_{la}, i_{lb}, i_{lc}) represents the three phase load currents, ($v^*_{ta1}, v^*_{tb1}, v^*_{tc1}$) represents the three phase source voltages, P_l is the average load power, P_{loss} represents the switching and ohmic losses in the actual compensator. $\beta = \frac{\tan \Phi}{\sqrt{3}}$. Φ is the desired phase angle between source voltage and current. In order to obtain unity power factor (UPF), the value of β was chosen as zero.

Average load power (P_l) is given by the equation,

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$$P_l = \frac{1}{T}\int_{t_1-T}^{t_1}(V_{sa}i_{la} + V_{sb}i_{lb} + V_{sc}i_{lc})\,dt \qquad (9)$$

Equation (8) shows the reference filter currents. It is applicable for the compensation provided by only one DSTATCOM. But in this topology, compensation is provided by two DSTATCOMs. Hence the ISCT equation (8) can be modified as,

$$i^*_{f1(abc)} = \alpha i_{l(abc)} - \alpha\left(\frac{v^+_{t(abc)1}}{\sum_{j=a,b,c} v^{+2}_{tj1}}\right)P_1 (10)$$

Equation (11) represents the reference filter currents of Inv1.

The reference filter currents of Inv2 is given by,

$$i^*_{f2(abc)} = (1-\alpha)i_{l(abc)} - (1-\alpha)\left(\frac{v^+_{t(abc)1}}{\sum_{j=a,b,c} v^{+2}_{tj1}}\right)P_1 \qquad (11)$$

Where α denotes the fraction of load compensation done by Inv1.

V. SIMULATION RESULTS

The distorted three phase source voltages are first converted to αβ0 transformation. Then it is again converted to dq0 transformation. Then the varying dq0 axis components are converted into a constant dq0 components by means of Moving Average Filter (MAF). Then this constant dq0 axis components are converted into abc axis where the fundamental positive sequence voltages are extracted and these voltages are used for the reference filter current generation. The 'ωt' used for the transformation is given by three phase Phase Locked Loop (PLL) block.

Table 1 System parameters

Parameters	Values
Grid Voltage	400 V L–L (rms), 50 Hz
Feeder Impedance	R_s = 0.5 Ω, L_s = 3mH
VSIs (Inv1 and Inv2)	dc capacitor, C_{dc} = 2200 μF neutral capacitor, C_n = 150 μF interfacing inductor, L_f = 10mH inductor resistance, R_f = 0.5 Ω hysteresis band (± h) = 5% of the compensator current
Voltage Controller PI gains	K_{pv} = 100, K_{iv} = 0.1
DC link voltage	$V^*_{dc} = 2V_{dc}$ = 1040 V
Unbalanced Linear Load	Zla = 17.5 + j7.8V, Zlb = 27.5+j12.5 Ω, Zlc = 37.5 + j31.4 Ω
Non- linear load	3-ϕ diode bridge rectifier with R = 20 Ω, L = 200 mH

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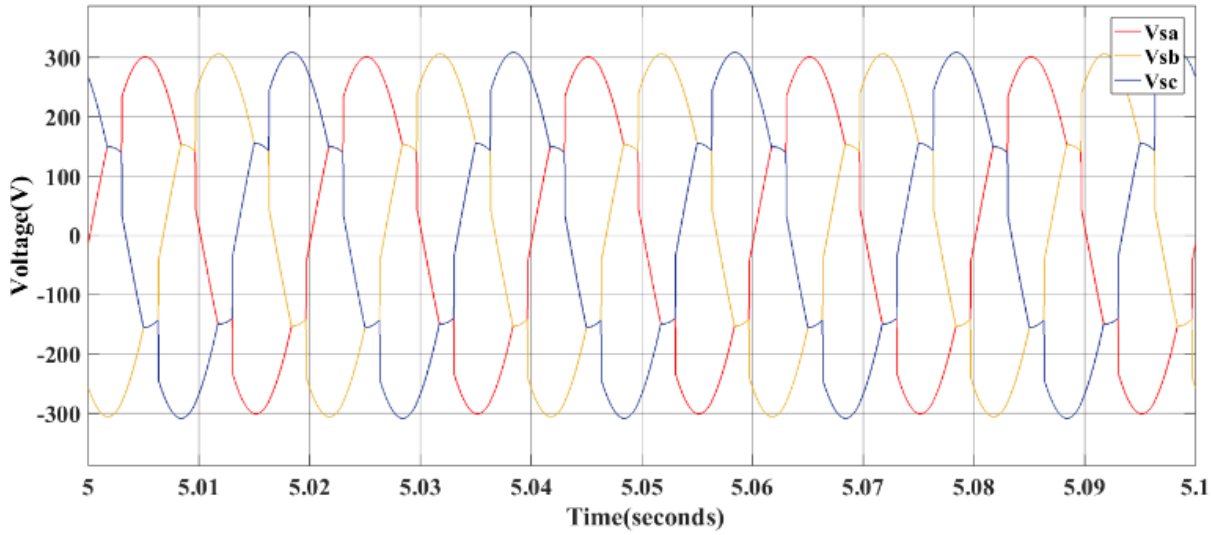

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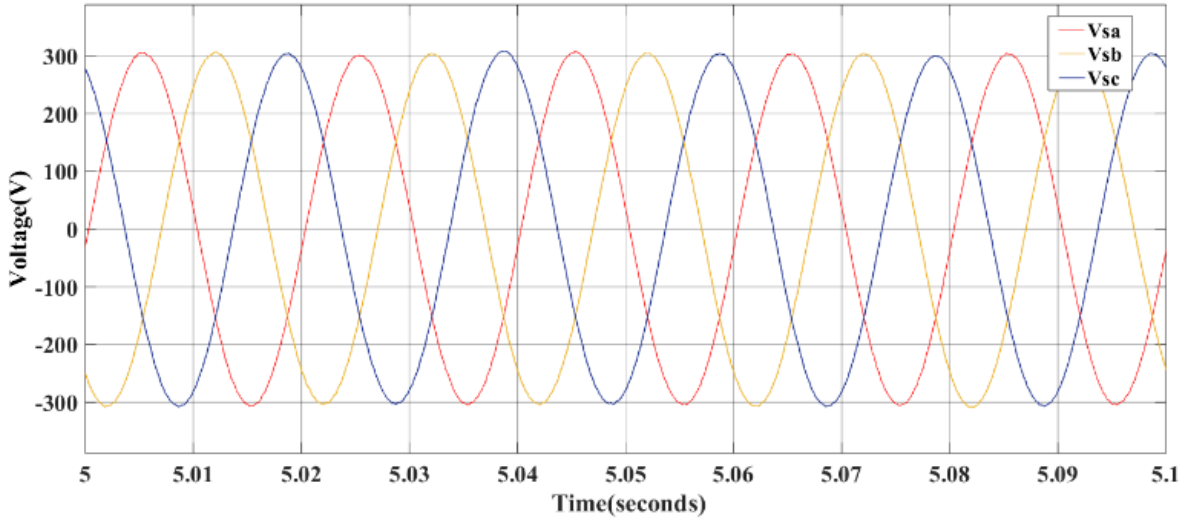

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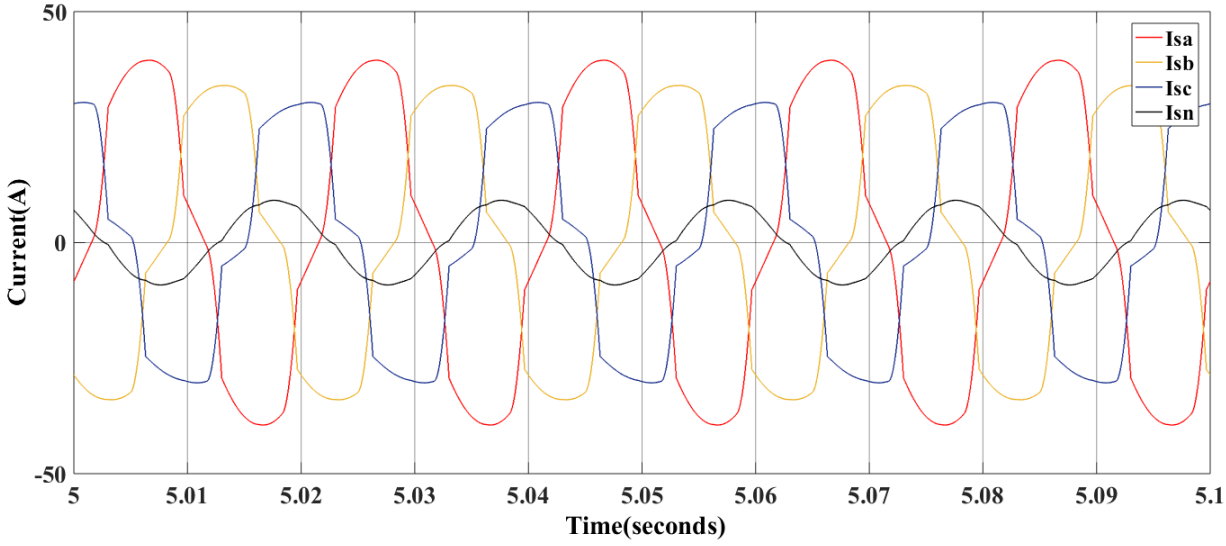

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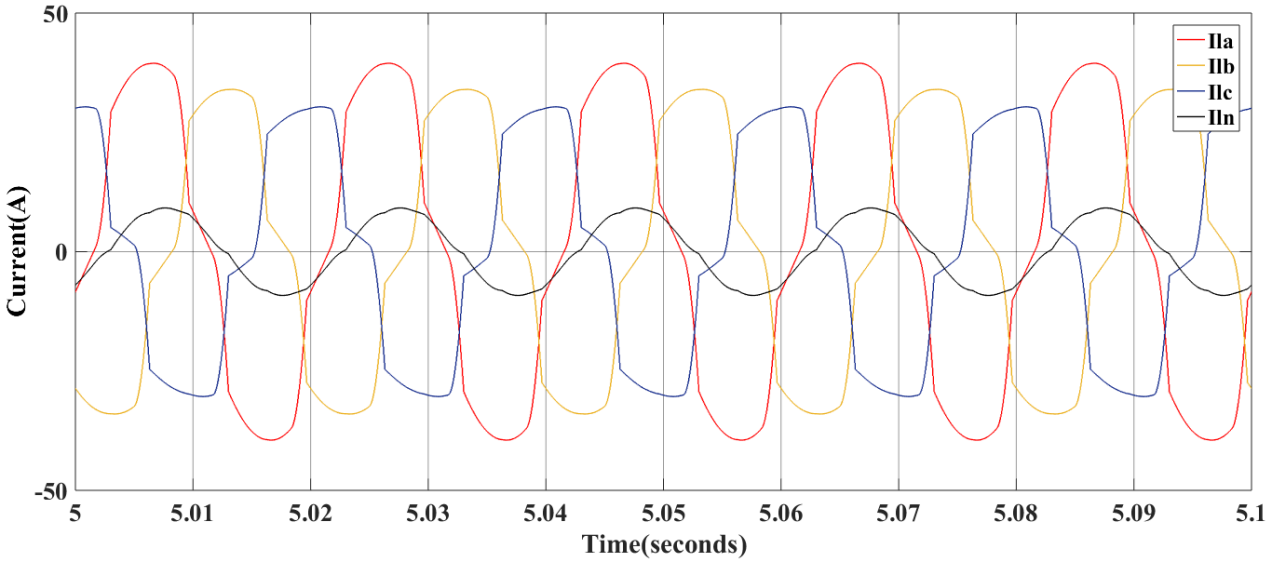
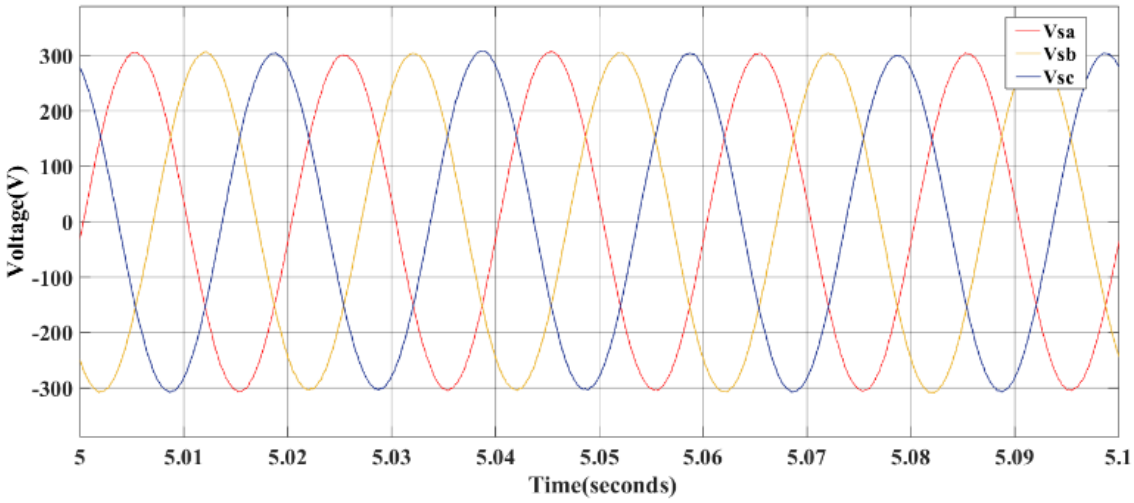


(d)

Fig 2 Steady state performance of dual DSTATCOM before compensation

Figure 2(a) shows the distorted three phase PCC voltages. It is due to the presence of feeder impedance on the line. Figure 3(b) shows the positive sequence of PCC voltages. It is obtained by the transformation techniques. The distorted PCC voltages cannot be able to generate the reference filter or compensator current. So, the distorted PCC voltages are converted into sinusoidal PCC voltages with equal magnitude and phase difference by means of transformation techniques.

Figure 2(c) shows the distorted three phase source currents (i_{sa}, i_{sb}, i_{sc}) before using any of the compensation techniques. Due to the unbalance present in the three phase source currents the neutral source current (i_{sn}) starts flowing through the line. This will overload the neutral conductor. The purpose of the DSTATCOM is to balance the distorted source currents and to bring the source neutral current to zero so as to perform the load balancing in the system. Figure 2(d) shows the distorted three phase load currents (i_{la}, i_{lb}, i_{lc}) due to the usage of linear unbalanced load and non-linear load (three phase diode bridge rectifier).



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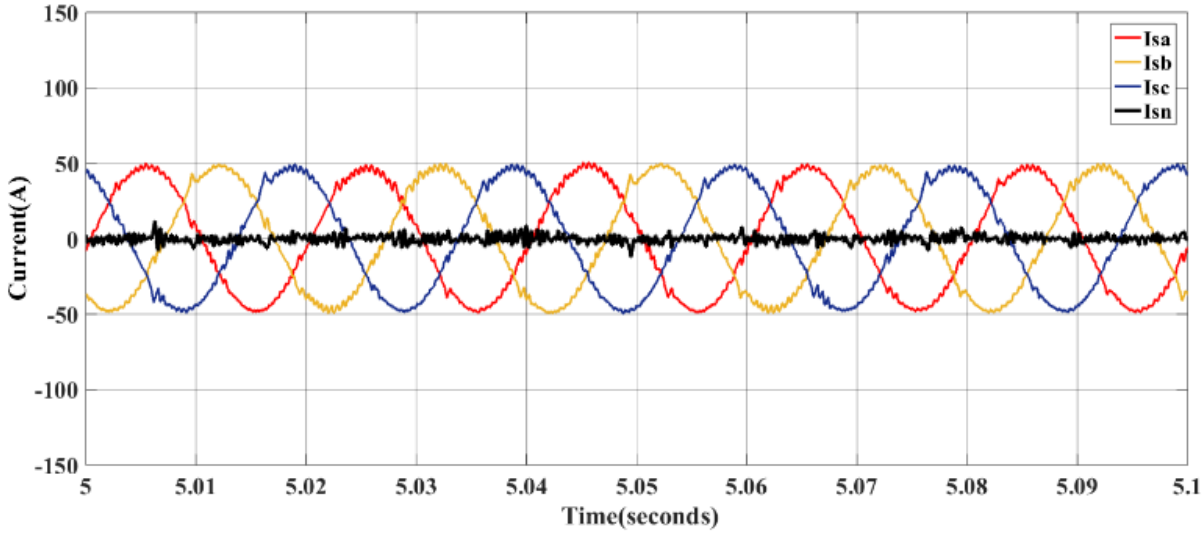

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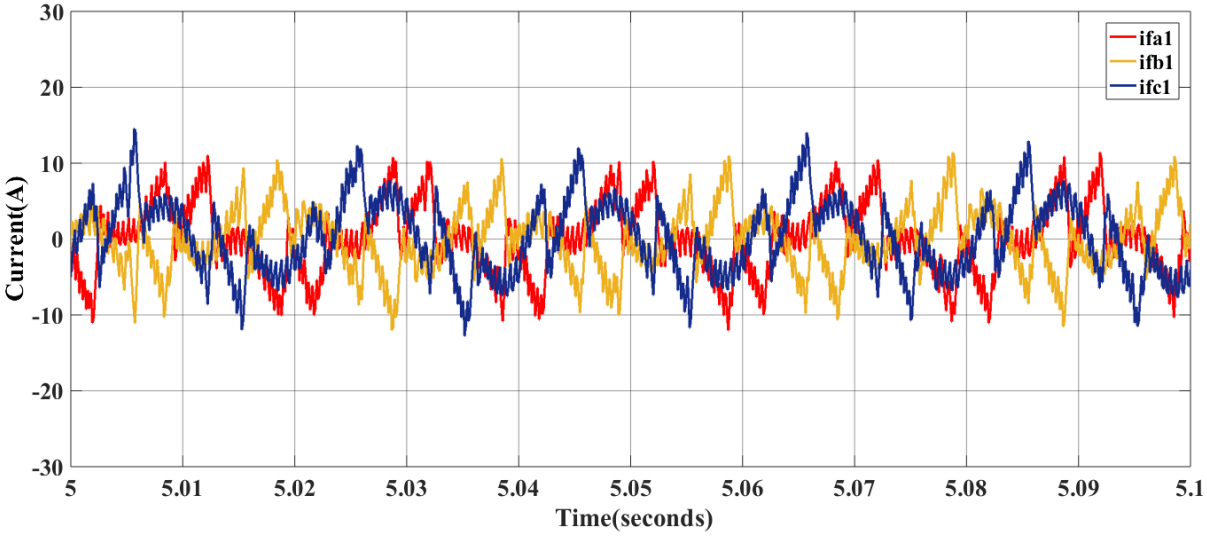

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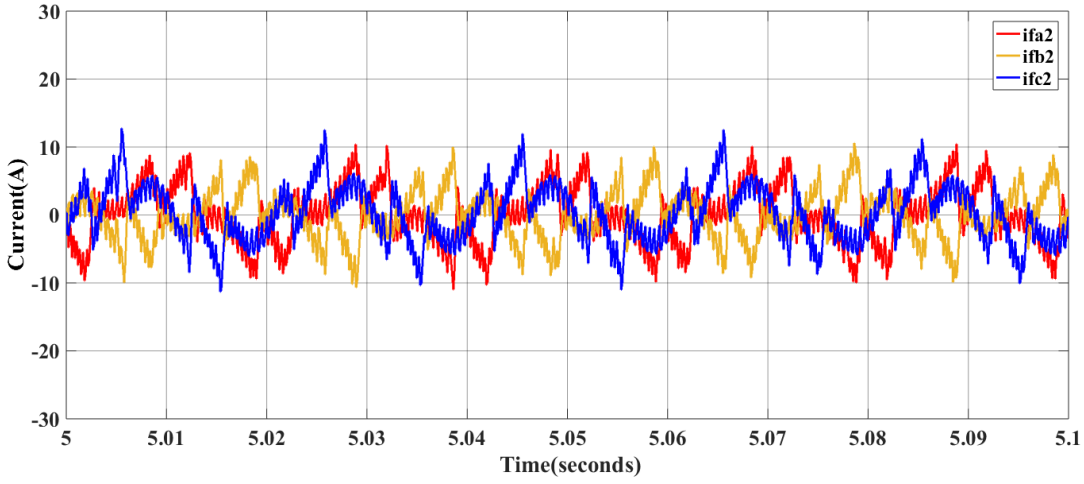

(d)

Fig 3 Steady state performance of dual DSTATCOM after compensation

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Figure 3(b) shows the three phase source currents (i_{sa}, i_{sb}, i_{sc}) after the compensation provided by the Dual DSTATCOM. In order to bring the source currents as balanced sinusoidal one, the compensator currents from Inv_1 and Inv_2 are injected into the line by means of an interfacing inductor. Source currents after compensation has equalmagnitude and properphase displacement between each other. At the same time the source neutral current (i_{sn}) also limited to zero.

Figure 3(c) shows the three phasecompensator or filter currents (if_{a1}, if_{b1}, if_{c1}) injected by the Inverter1 (DSTATCOM) in order to compensate the unbalance present in the three phase source currents. The pulses for the Inv_1 is given by the control algorithm techniques. Figure 3(d) shows the three phase compensator or filter currents (if_{a2}, if_{b2}, if_{c2}) injected by the Inverter2 (DSTATCOM) in order to compensate the unbalance present in the three phase source currents. The pulses for the Inv_2 is given by the control algorithm techniques.

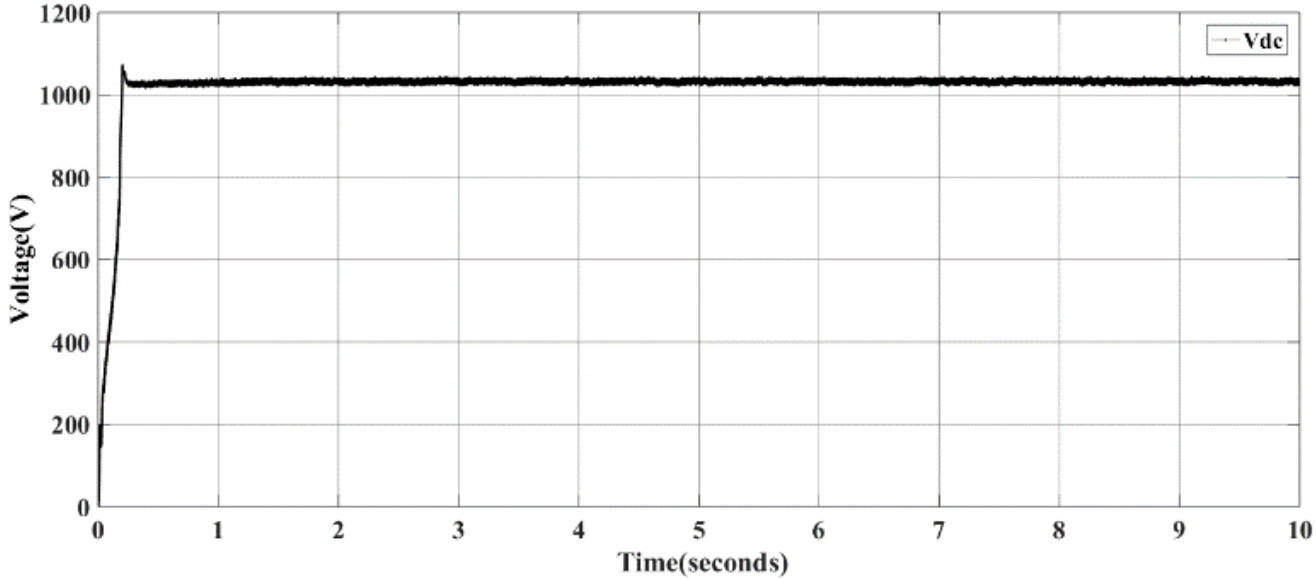
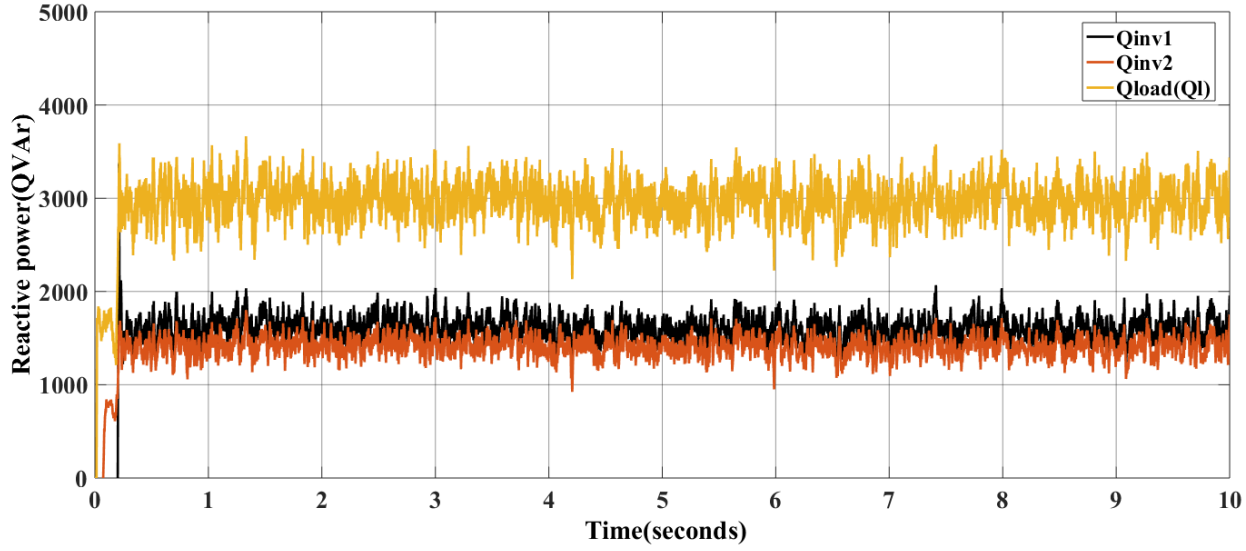


Fig 4 DC link voltage (V_{dc}) across the dc link capacitor

Figure 4 shows the DC link voltage (V_{dc}). It is maintained constant with the help of PI controller used in the system. In this paper, the dc-link voltage is maintained by only one inverter (Inv_1).



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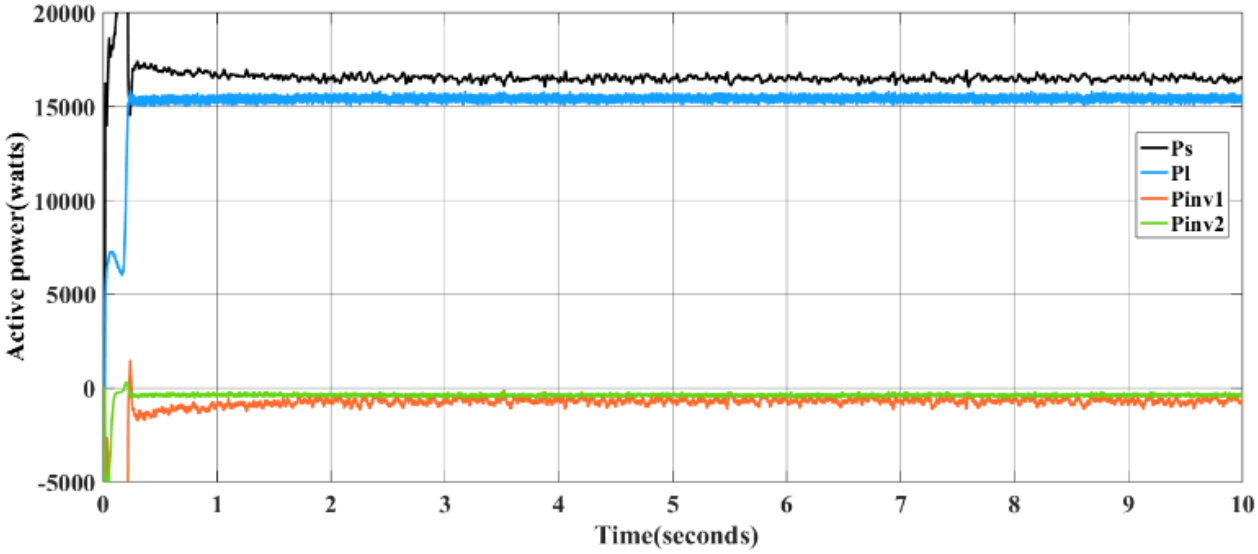

(b)

Fig 5 Power sharing of dual DSTATCOM topology

Figure 5(a) shows the reactive power sharing between the two inverters (Inv_1 and Inv_2). The rated KVA capacity of two inverters (S_1 and S_2) is taken as 8 KVA for Inv_1 and 7 KVA for Inv_2. The α value is designed by the value of S_1 and S_2. It is formed by the equation (16). Therefore, the reactive power requirement of load is partially divided between the two inverters which means that (Reactive power of load = Reactive power supplied by Inv_1 + Reactive power supplied by Inv_2).

Figure 5(b) shows the active power sharing between source, load and both the inverters (Inv_1 and Inv_2). The active powers of both Inv1 and Inv2 is nearly zero, which indicates that the DSTATCOM does not use the active power for compensation. It uses only the reactive powers of Inv1 and Inv2. Hence it is called as Reactive power compensation. The figure also shows that the active power of source (P_s) is almost equal to the active power of load (P_l) after compensation which means that the source side and load side are almost balanced after the compensation.

As per IEEE standard for Power Quality the Total Harmonic Distortion (THD) of a particular waveform must be less than 5% . Therefore, the THD level is more than 5% for the source currents in case of before compensation. But in the case of after compensation technique, the level of THD for all the three source currents (I_{sa},I_{sb},I_{sc}) is less than 5% . So it can be acceptable as per the standards of IEEE.

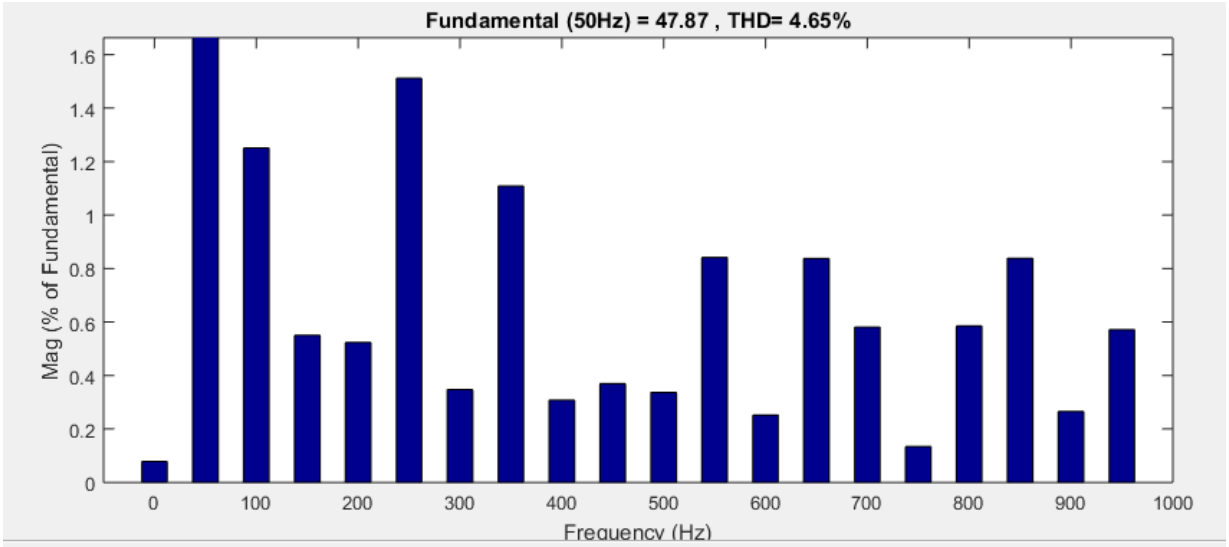

Fig 6 Harmonic spectrum of phase 'c' in Dual DSTATCOM structure with Single DC link capacitor

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VI. CONCLUSION

The performance of dual DSTATCOM topology for three phase four-wire distribution systems is explained with simulation results. Since, the dual DSTATCOM is used for compensation it reduces the ratings of the switches, dc link capacitor and also reduces the stress across the VSI switches. It also has the ability to share the reactive powers between the two VSIs. In this topology, the voltage unbalancing issue present in the split capacitor based topology is avoided due to the usage of common dc link between the two VSIs. It also has better harmonic elimination, power factor improvement and load balancing when compared to other DSTATCOM topologies.

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